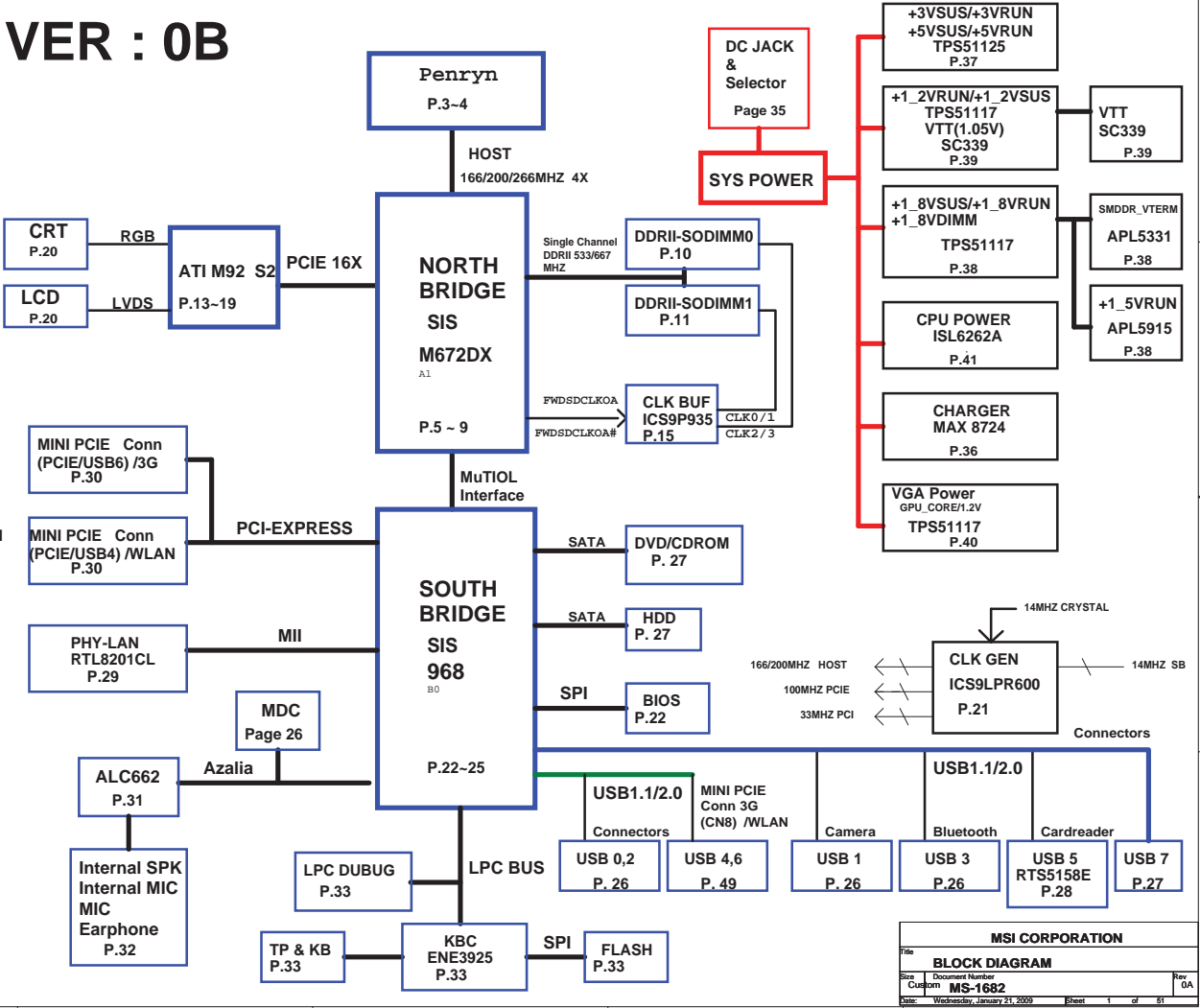


MS-1682 VER : 0B

- 01_BLOCK DIAGRAM
- 02_PLATFORM
- 03_PENRYN-1 (HOST BUS)
- 04_PENRYN-2 (POWER/GND)
- 05_M672DX-1 (HOST BUS & PCIE)
- 06_M672DX-2 (MutIO)
- 07_M672DX-3 (DDR2)
- 08_M672DX-4 (POWER)
- 09_M672DX-5 (VSS)
- 10_DDR2 SODIMM 0
- 11_DDR2 SODIMM 1
- 12_DDR2 TERMINATION
- 13_M92M-host-lvds
- 14_M92M-IO
- 15_M92M-power
- 16_M92M-power-straps
- 17_M92M_MEM Interface
- 18_M92M_DDR2_A0
- 19_M92M_DDR2_A1
- 20_CRT & LVDS CONN
- 21_CLOCK GEN & Dimm BUF
- 22_SIS968-1 (PCI/IDE/SPI/MutIO)
- 23_SIS968-2 (USB/SATA)
- 24_SIS968-3 (CPU/HD/PCIE/GPIO)
- 25_SIS968-4 (POWER/GND)
- 26_USBX2&Camera&MDC&BT CONN
- 27_HDD & ODD CONN & NEW CARD
- 28_RTS5158E_CARD READER
- 29_PHY LAN (RTL8201CL)
- 30_MINI_PCIECARD & LED & SW
- 31_AUDIO(ALC662) / AMP(APA2031)
- 32_SPK & HP & MIC
- 33_KBC/EC/uP (ENE3925)
- 34_PWRGD & FAN & C3/C4
- 35_Battery select
- 36_Battery Charger
- 37_M_System Power
- 38_M_1.8V & SMDDR_VTERM & 1.5V
- 39_M_1.2V & VTT power
- 40_VGA power
- 41_CPU power
- 42_Screw
- 43_EMI
- 44_Power Sequence-1
- 45_Power Sequence-2
- 46_Power Sequence_3
- 47_Launch Board
- 48_TP Board
- 49_USBx2 & RJ45 & RJ11 Board



MSI CORPORATION			
BLOCK DIAGRAM			
File	Document Number	Rev	0A
Size	Custom	MS-1682	
Date	Wednesday, January 21, 2009	Sheet	1 of 51

Voltage Rails

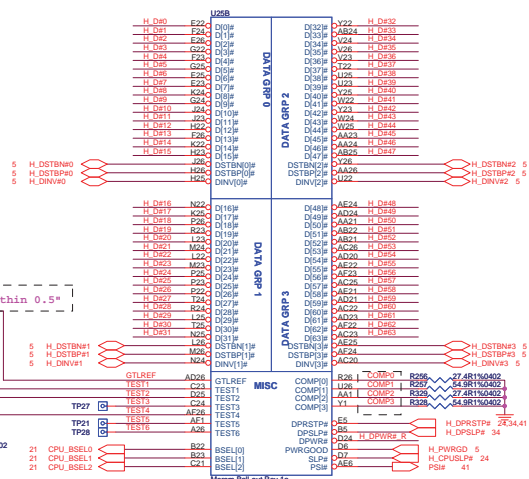
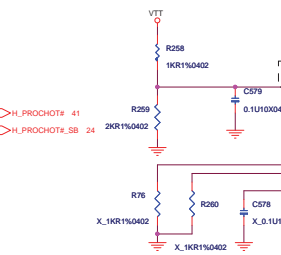
Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
V_CORE	Core Voltage for Processor	VR_ON
+VTT	1.05 rail for Processor & SIS968 GTL IO	+1_5VM_PG
+1_5VRUN	1.5V switched power rail(off in S3-S5)	+5VRUN
+1_2VRUN	1.2V power rail SISM672FX Analog (off in S3-S5)	RUND (RUN_ON)
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND (RUN_ON)
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND (RUN_ON)
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	RUN_ON
+1_8VDIMM	1.8V power rail DDRII (off in S4-S5)	DIMM_ON
+1_8VRUN	1.8V power for SIS968 MuTIOL IO and core logic (off in S3-S5)	RUND (RUN_ON)
+1_8VSUS	1.8V power rail for SB core logic (off in S4-S5)	SUS_ON
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	RUND
+1_2VSUS	1.2V power rail SISM672FX Digital (off in S4-S5)	SUS_ON

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks	+1_8VDIMM
Full ON	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW	ON
S3(Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF	ON
S4(Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	ON	OFF	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

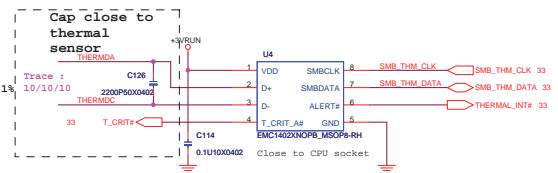
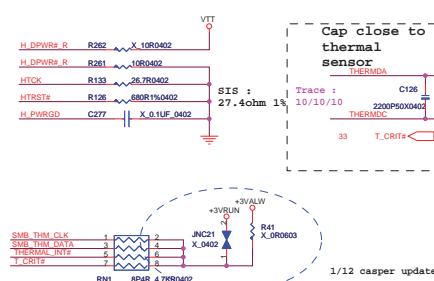
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Title			
PLATFORM			
Size	Document Number		Rev
Custom	MS-1682		0A
Date:	Wednesday, January 21, 2009		Sheet 2 of 51



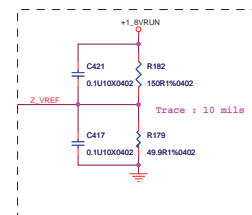
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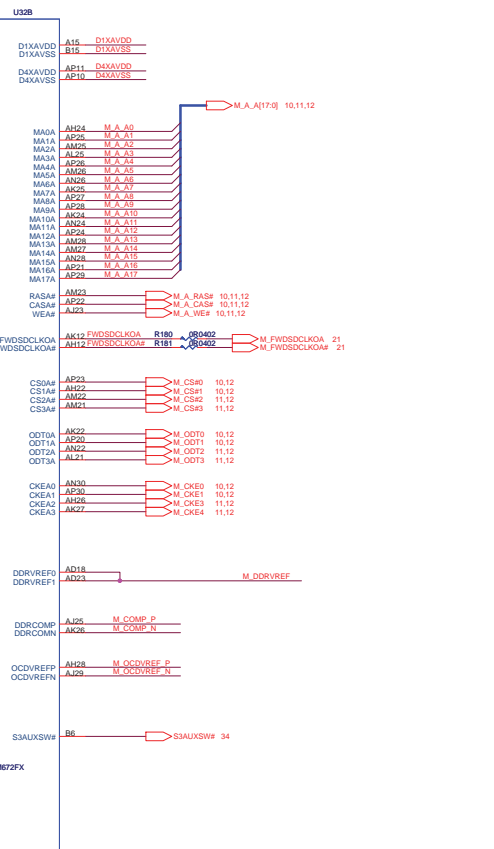
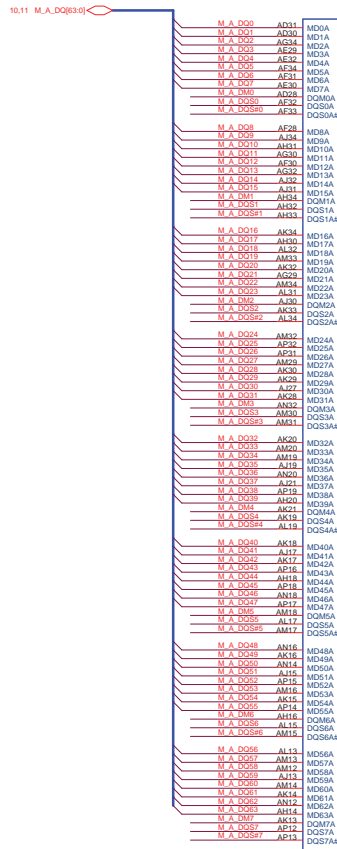
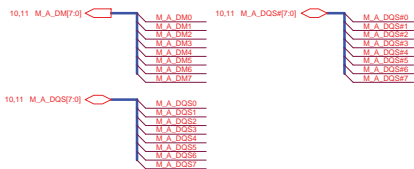
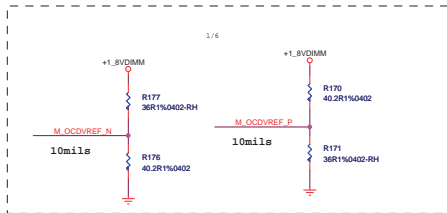
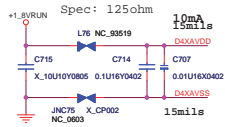
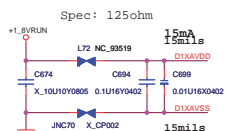
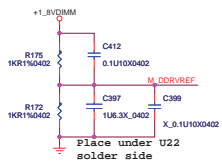
| Within 0.5"
| 25mils Spacing
| COMP0,2 --> 18mils
| COMP1,3 --> 5mils

```





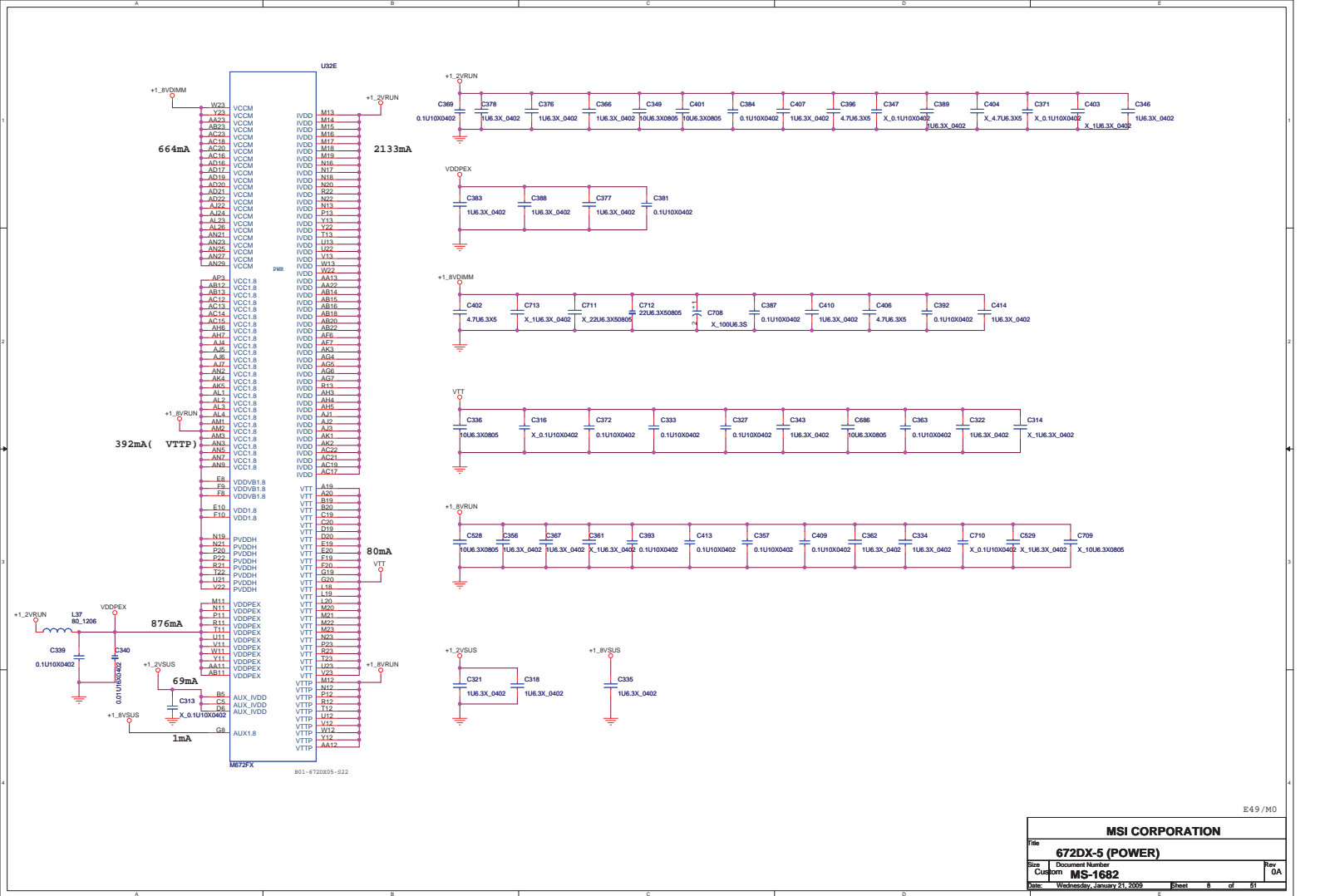


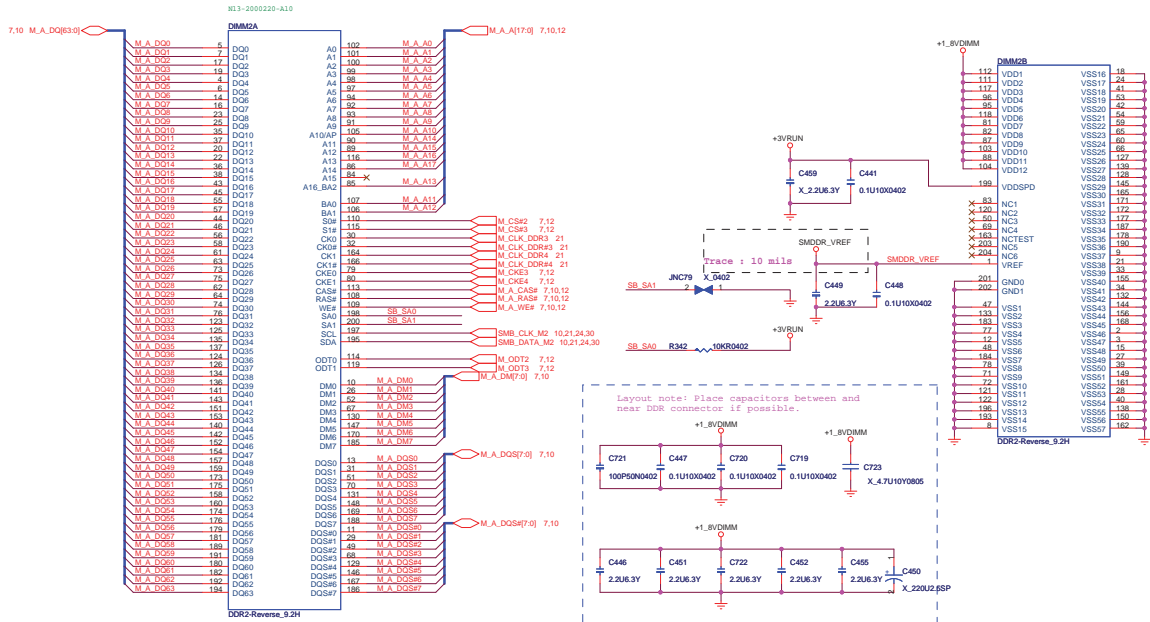


801-672035-522

E17/M0

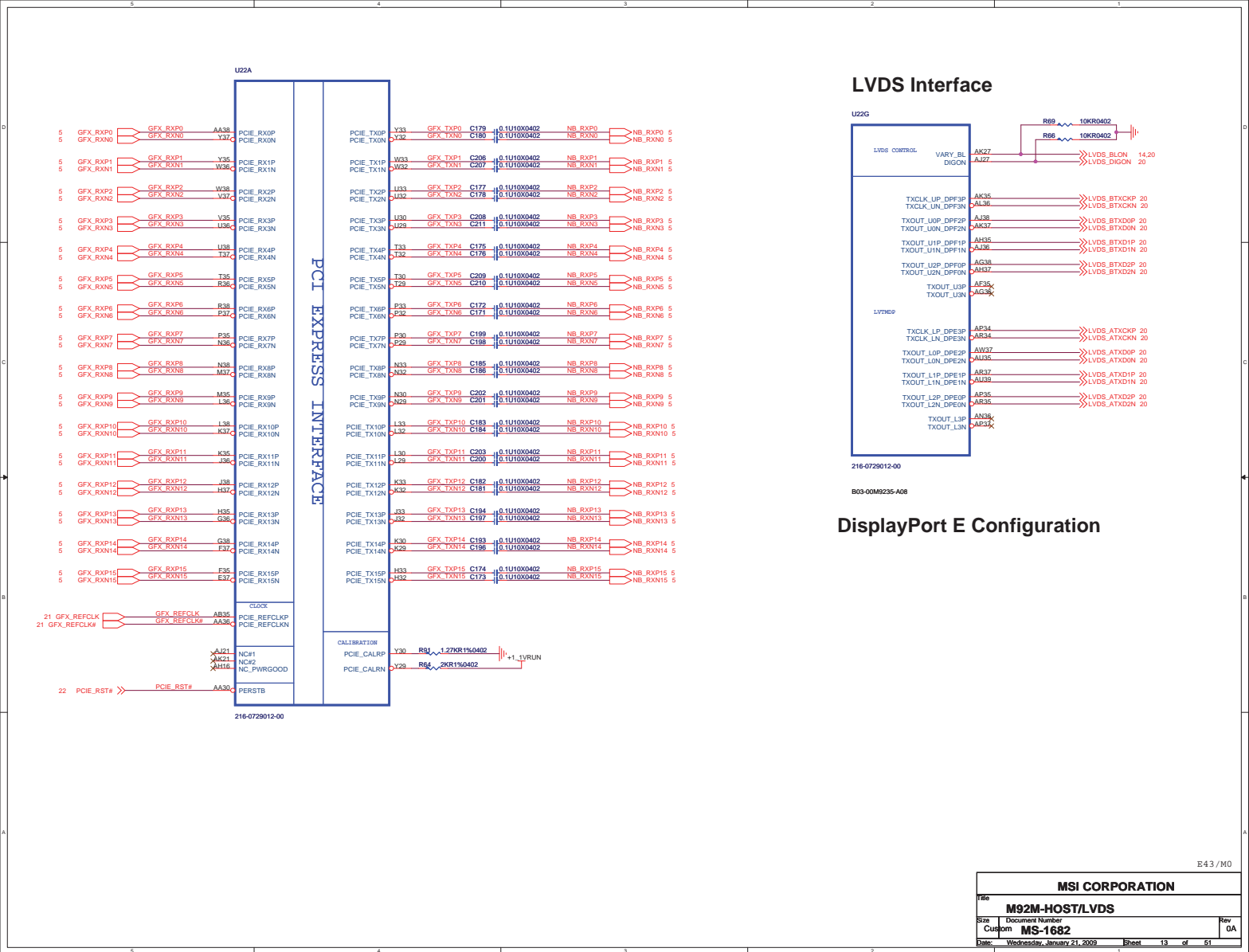
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Size	Document Number	Rev	
Custom	MS-1682	0A	
Date	Wednesday, January 21, 2009	Sheet	7 of 51



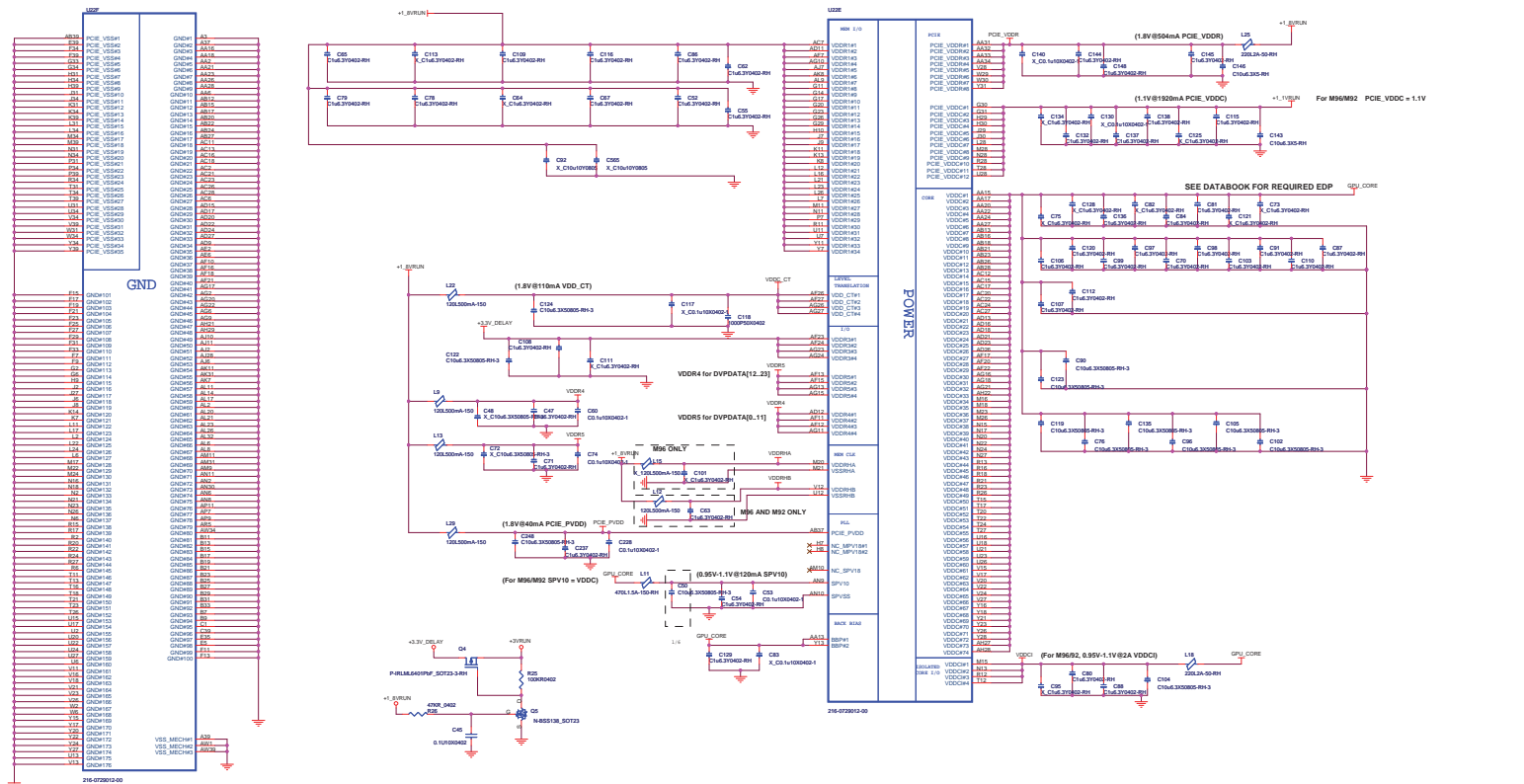


E12/M0

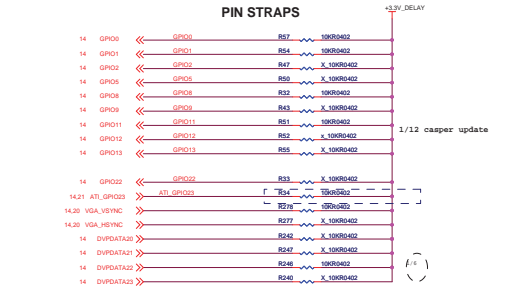
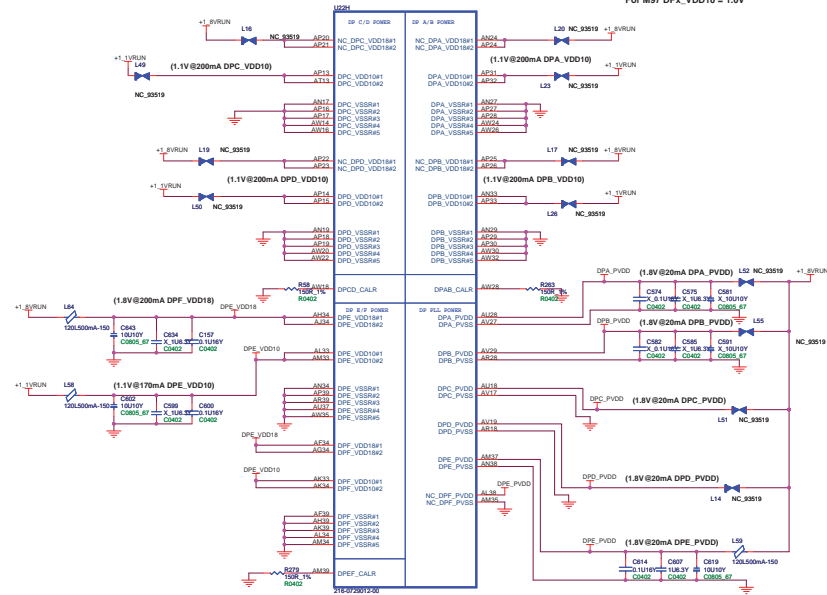
MSI CORPORATION			
File	DDR2 SODIMM 1		
Size	Document Number	Rev	0A
Custom	MS-1682		
Date	Wednesday, January 21, 2009	Sheet	11 of 51







For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V



CONFIGURATION STRAPS			RECOMMENDED SETTINGS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GP0S ARE USED, THEY MUST NOT CONFLICT DURING RESET			DO NOT INSTALL RESISTOR I = INSTALL 10K RESISTOR L = DESIGN DEPENDENT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_EN	GP00	Transmitter Power Savings Enable 0=ON, Tx output saving for mobile mode 1=Full Tx output saving (default setting for desktop)	1
TX_DEEMPH_EN	GP01	PCI Express Transmitter Deemphasis Enable 0=Tx de-emphasis disabled for mobile mode 1=Tx de-emphasis enabled (default setting for desktop)	1
BIF_GEN2_EN	GP02	0 = Advertises the PCI-E device as 2.0 GT/s capable at power-on 1 = Advertises the PCI-E device as 3.0 GT/s capable at power-on 2.0 GT/s Capability will be controlled by	0
STRAP_BIF_CLK_PAL_EN	GP08	Enables CLKREQ# Power Management 0 = CLKREQ# Power Management capability is disabled 1 = CLKREQ# Power Management capability is enabled	0
BIF_VGA_DIS	GP09	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GP021	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GP022, RMC38	Enables external BIOS ROM device 0 = disable external BIOS ROM device 1 = enable external BIOS ROM device	0
config2: 1, 0	GP013, 12, 11	GP0 0,13,12,11(CONFIG 3,2,1,0) a= If BIOS_ROM_EN=0, then Config(3) defines the rom type b= If BIOS_ROM_EN=0, then Config(3) defines the Aperture size	0 0 1 256MB 1/12 casper update
Mem type	DVGA2P021,22	If VFP_DEVICE_STRAP_EN is set to 'Y' then this pin is used to sense whether a VFP (non device) is connected to the VFP bus (interface to VFP_DEVICE_STRAP_EN is set to 'Y' then this pin is not used as a strap at all i.e. its value during reset is unimportant), and it can be used as a regular GP0D	0 0 0 vendor
VFP_DEVICE_STRAP_ENA	VS0VNC		0
RSVD	HS0VNC		0
AUD01	GEN0CC		0
AUD02	HS0VNC		1
	VS0VNC		1

DV DATA	23	22	21	20	
SAMSUNG	0	0	0	0	32*16
Hynix	0	0	0	1	32*16
SAMSUNG	0	0	1	0	64*16
Hynix	0	1	0	0	64*16

MSI CORPORATION

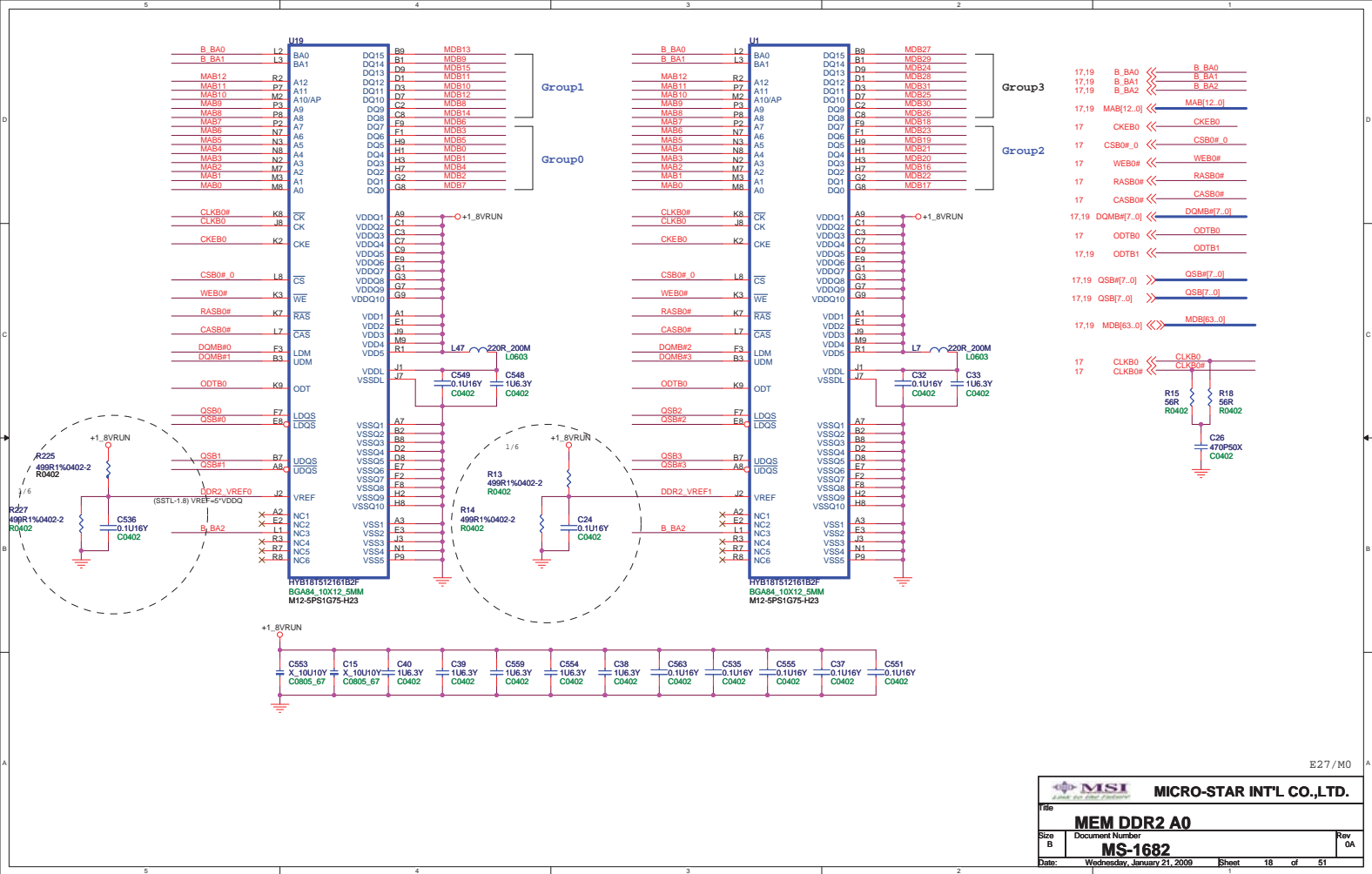
M92M-power straps

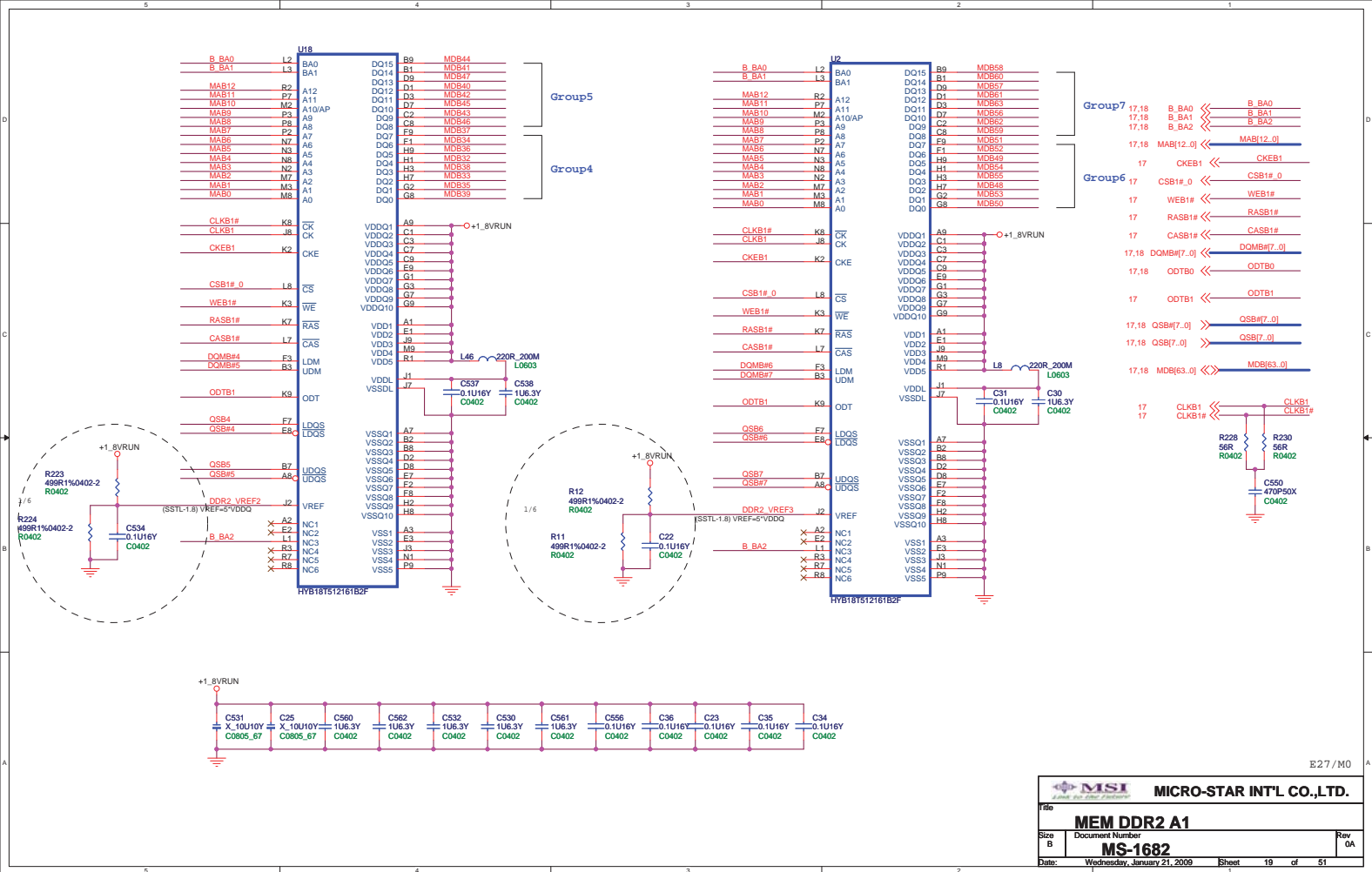
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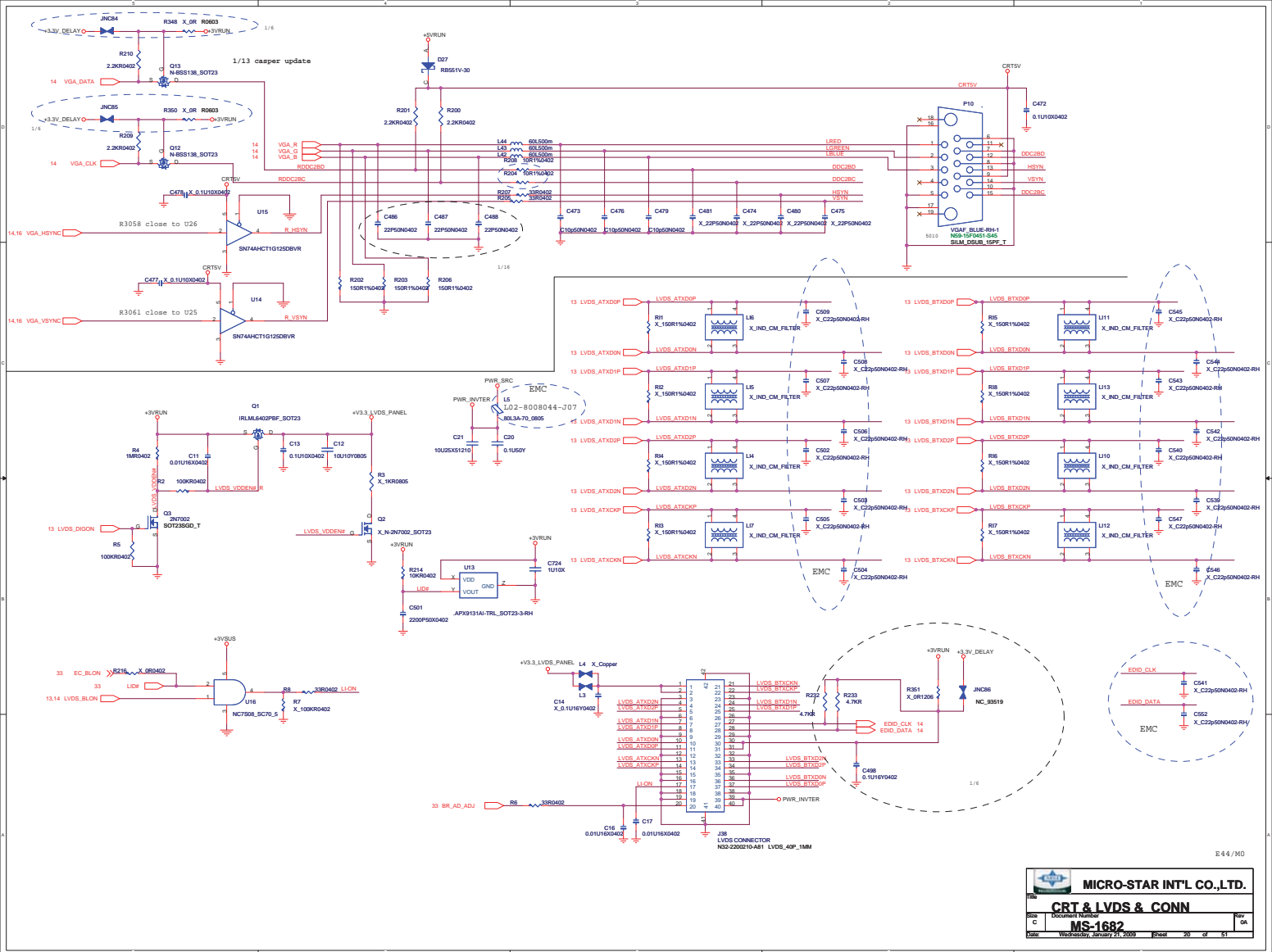
Ver: V1.00, January 21, 2005

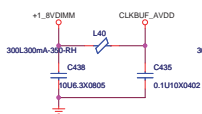
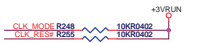
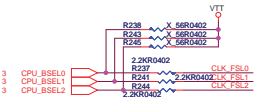
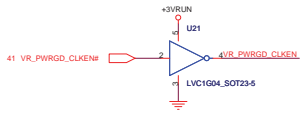
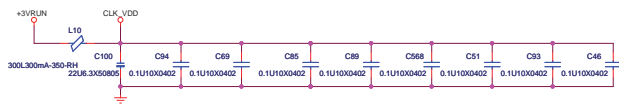
Page 18 of 51

GA







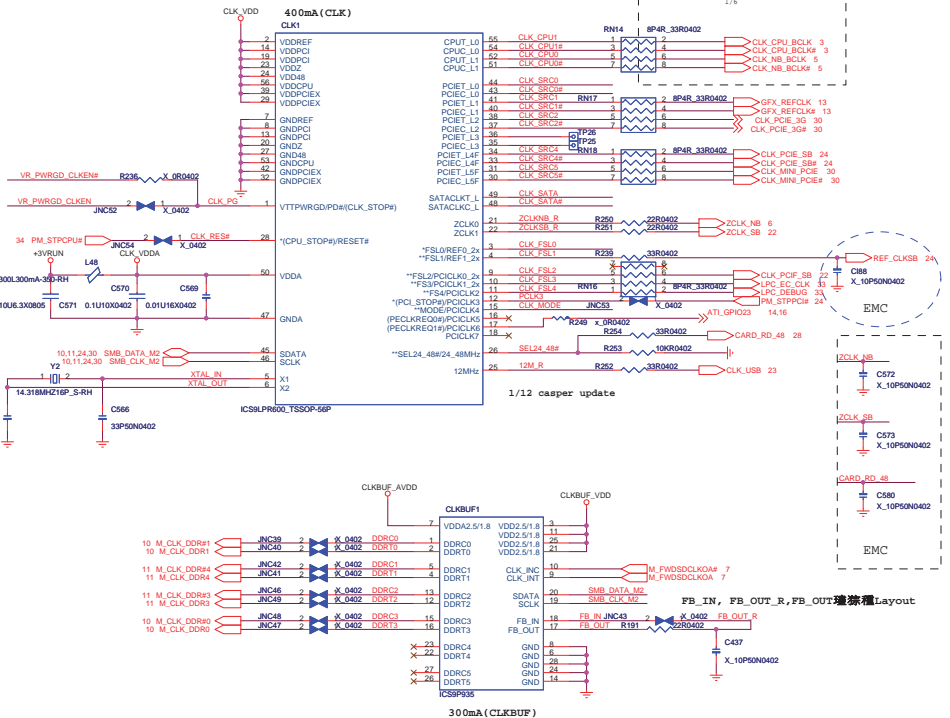
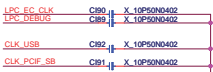


Strapping Configuration (IC5)

PIN#	High	Low (Default)
15	Pin 16/17 : PECLKREQ	Pin 16/17 : PCICLK

CPU Table				FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]		
L	H	H		667 MHz
L	H	L		800 MHz
L	L	L		1066 MHz

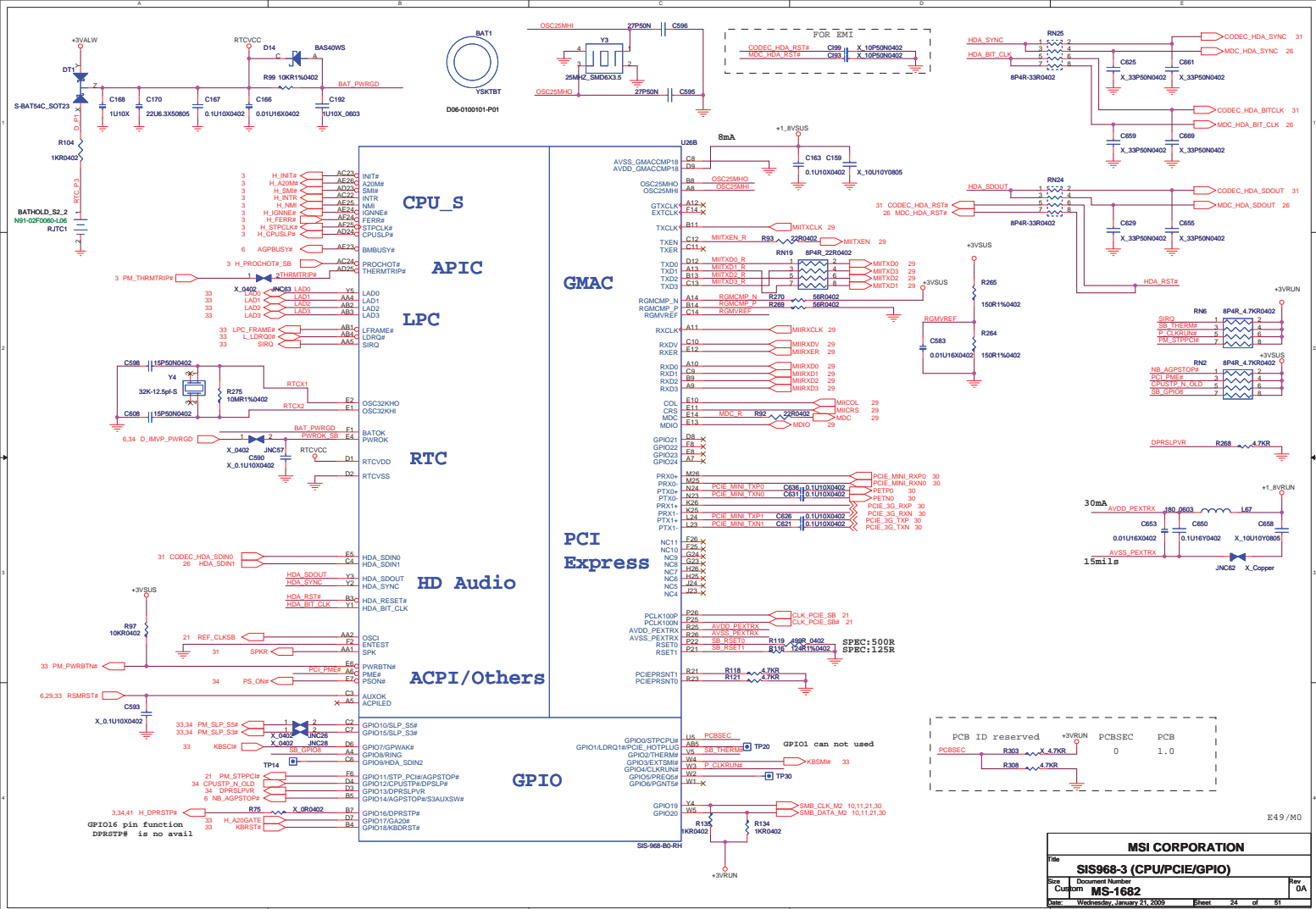
FOR EMI close to CLK1



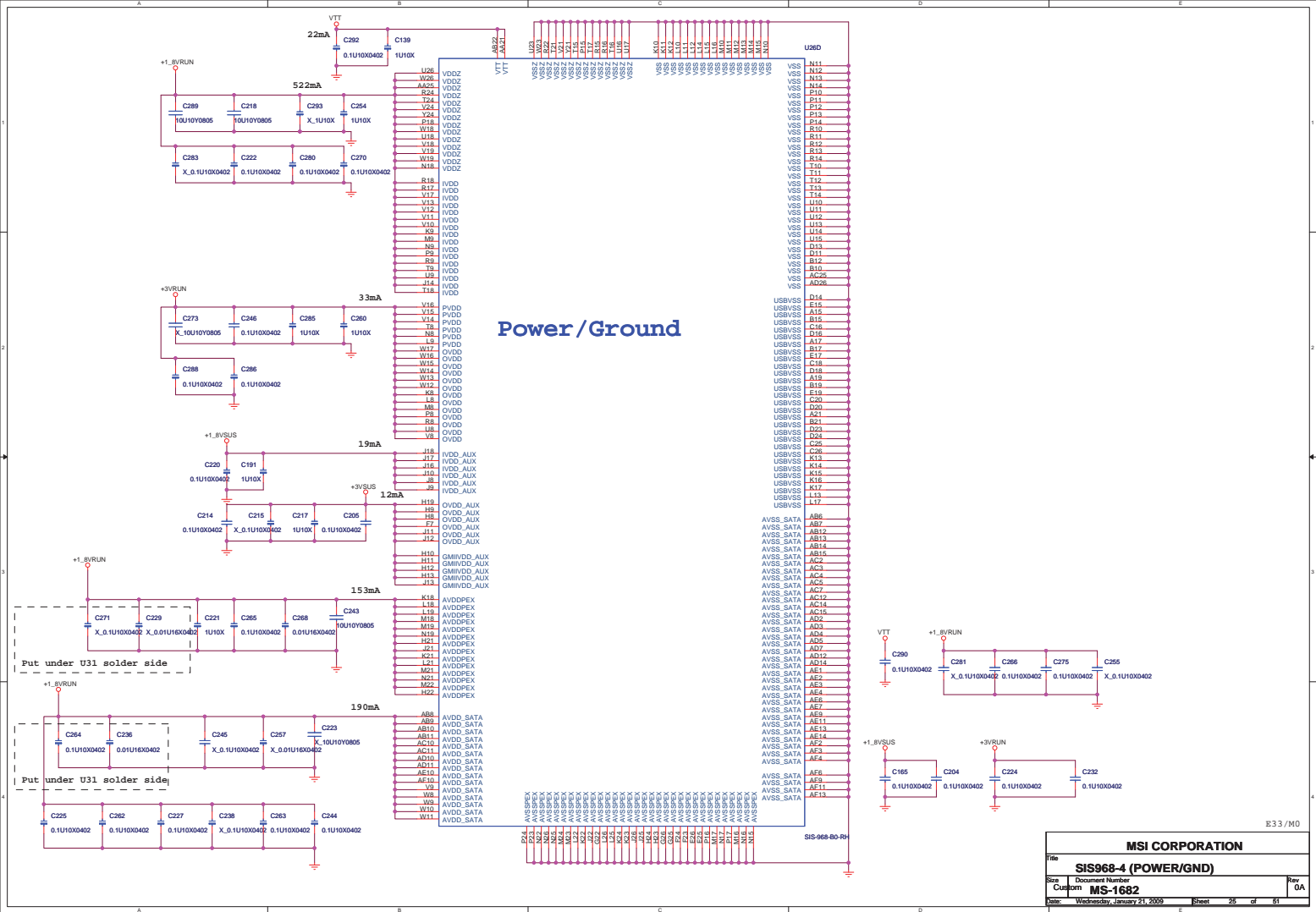
1/16 JNC39,40,41,42 +1.5" AND JNC43 +2"FOR 3D MARK 06 BUG ,

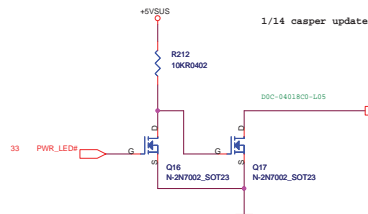
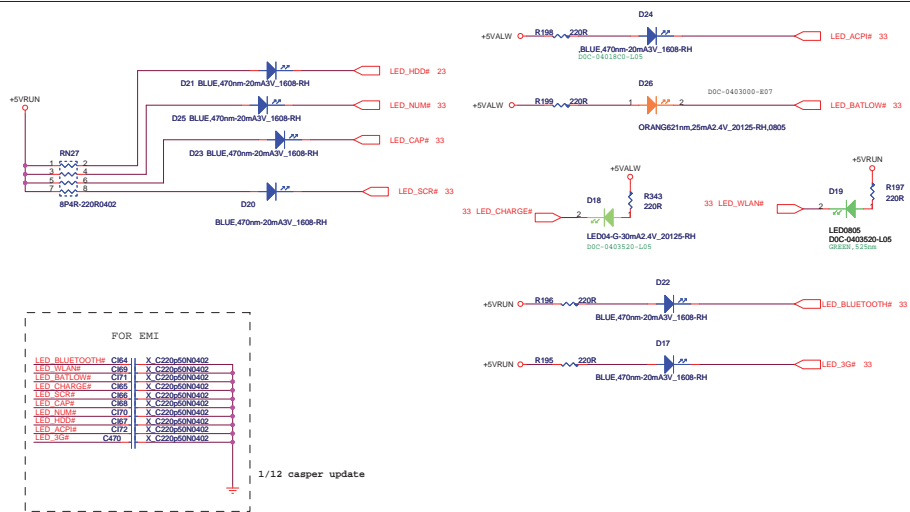
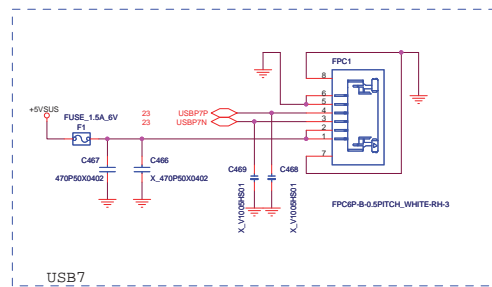
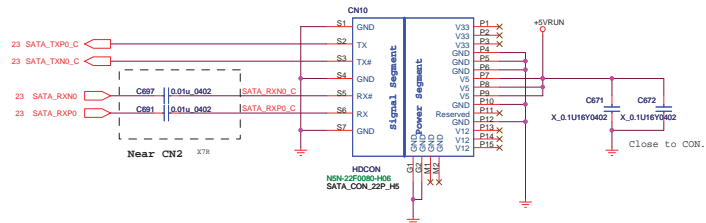
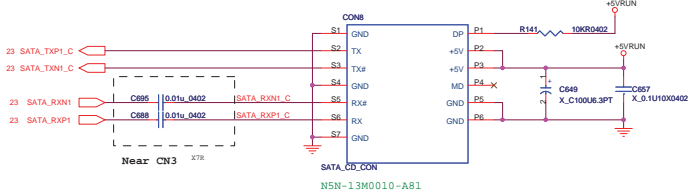
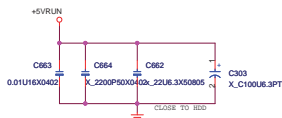
E45/M0

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Size: Custom	Document Number: MS-1682	Rev: 0A	
Date: Wednesday, January 21, 2009	Sheet: 21	of 51	



Power/Ground

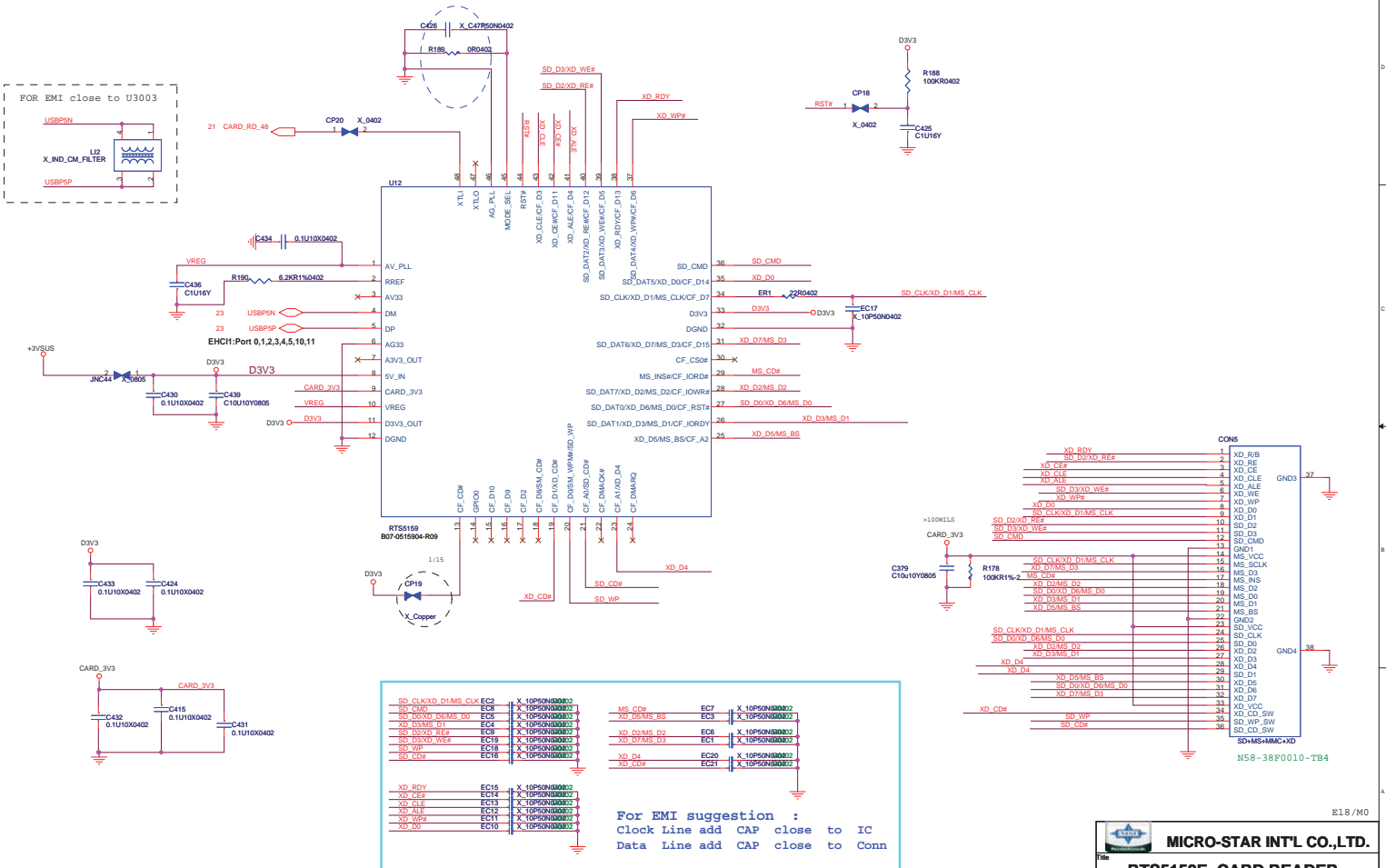




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Title: HDD & ODD CONN & USB7 & LED			
Size	Document Number	Rev	
Custom	MS-1682	DA	
Date	Wednesday, January 21, 2009	Sheet	27 of 51

E3.2/M0

FOR EMI close to U3003

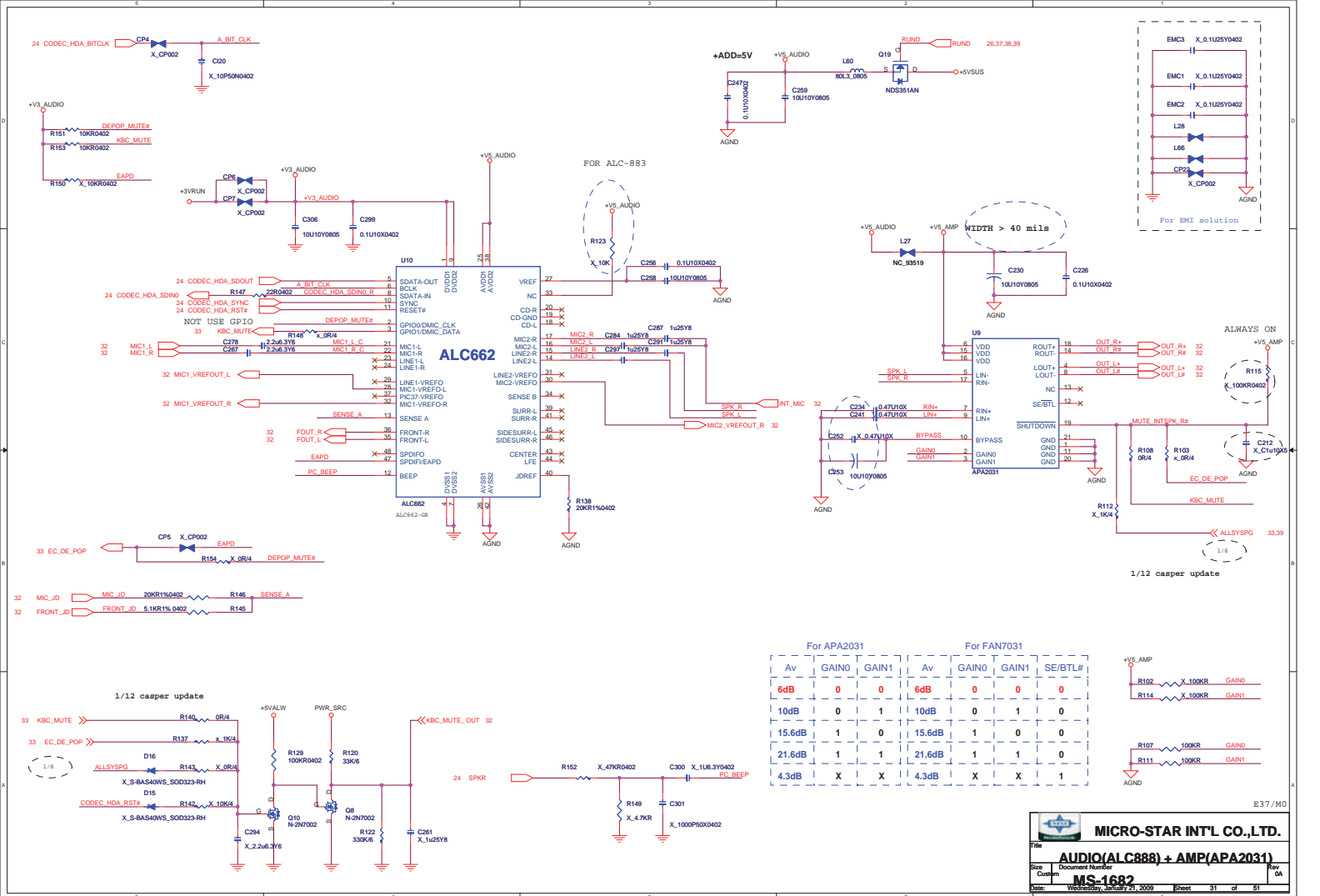


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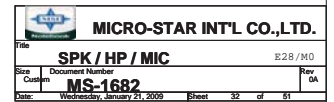
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RTS5158E CARD READER	
Size	Document Number
Customer	MS-1682
Date	Wednesday, January 21, 2009
Sheet	28 of 51

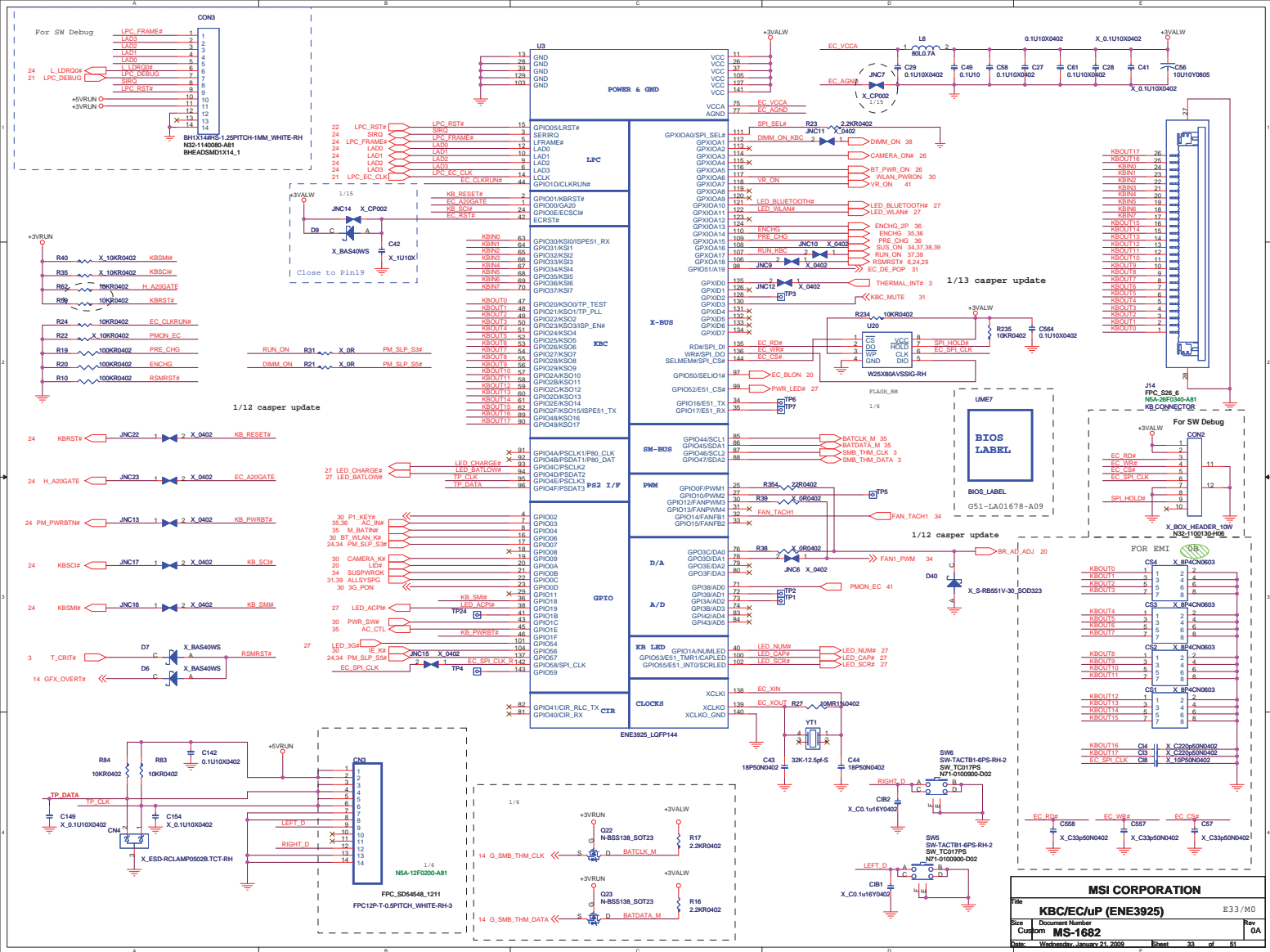
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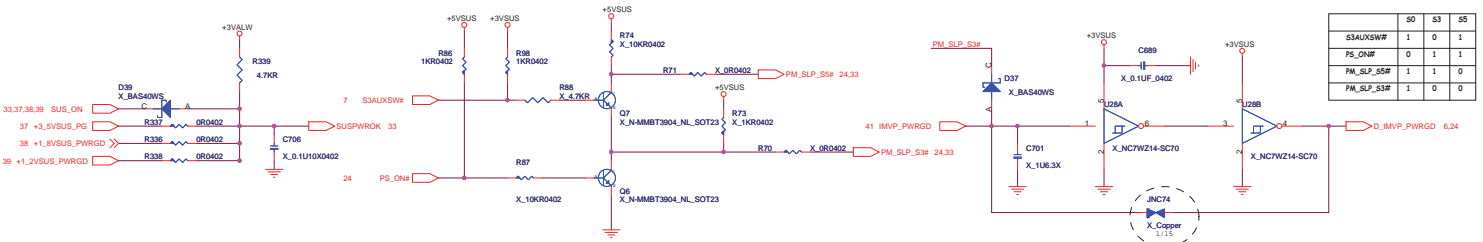
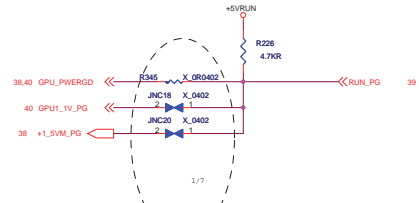
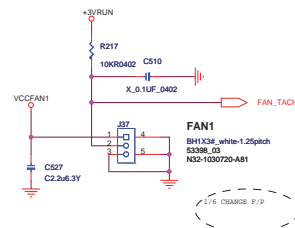
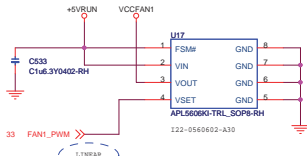


HP IN IS LOW

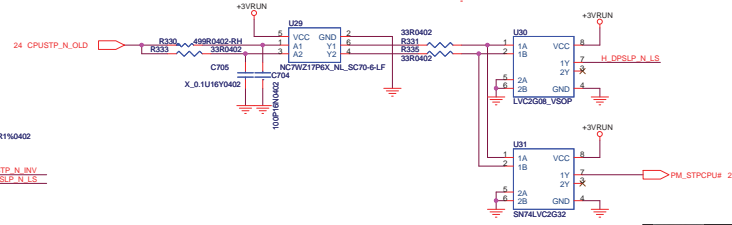
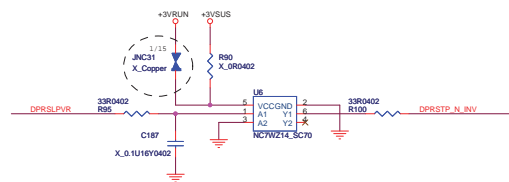
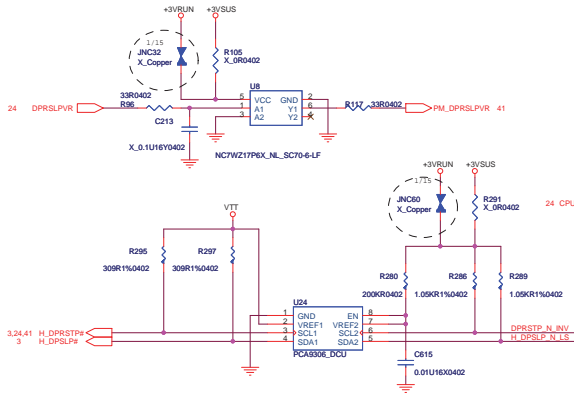




VCCFAN1=1.6+FAN1_PWM



	S0	S3	S5
S3AUXSW#	1	0	1
PS_ON#	0	1	1
PM_SLP_S#	1	1	0
PM_SLP_S#	1	0	0

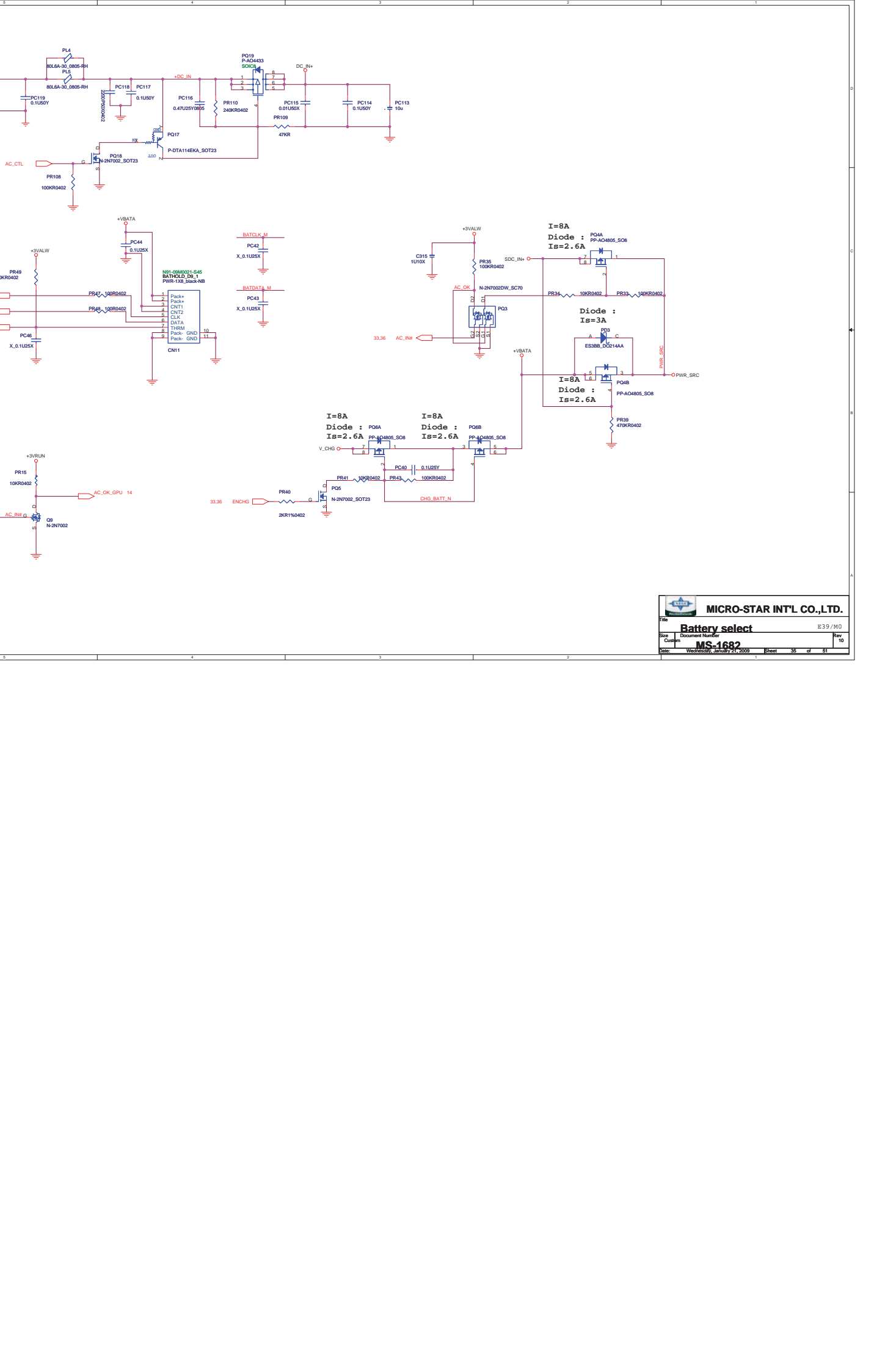


MICRO-STAR INT'L CO.,LTD.

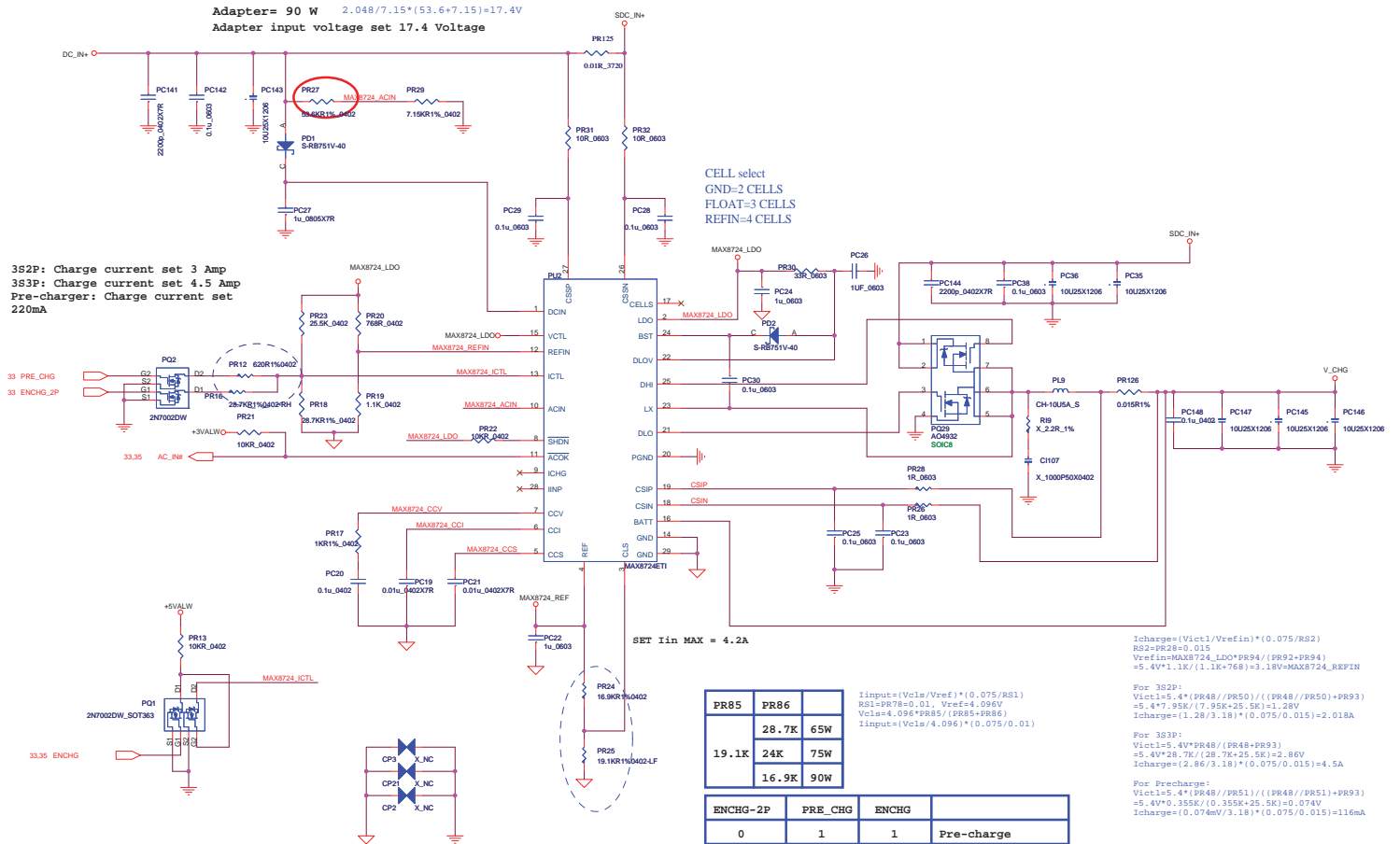
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Size: Custom Document Number: **MS-1682** Rev: DA

Date: Wednesday, January 21, 2009 Sheet: 34 of 51



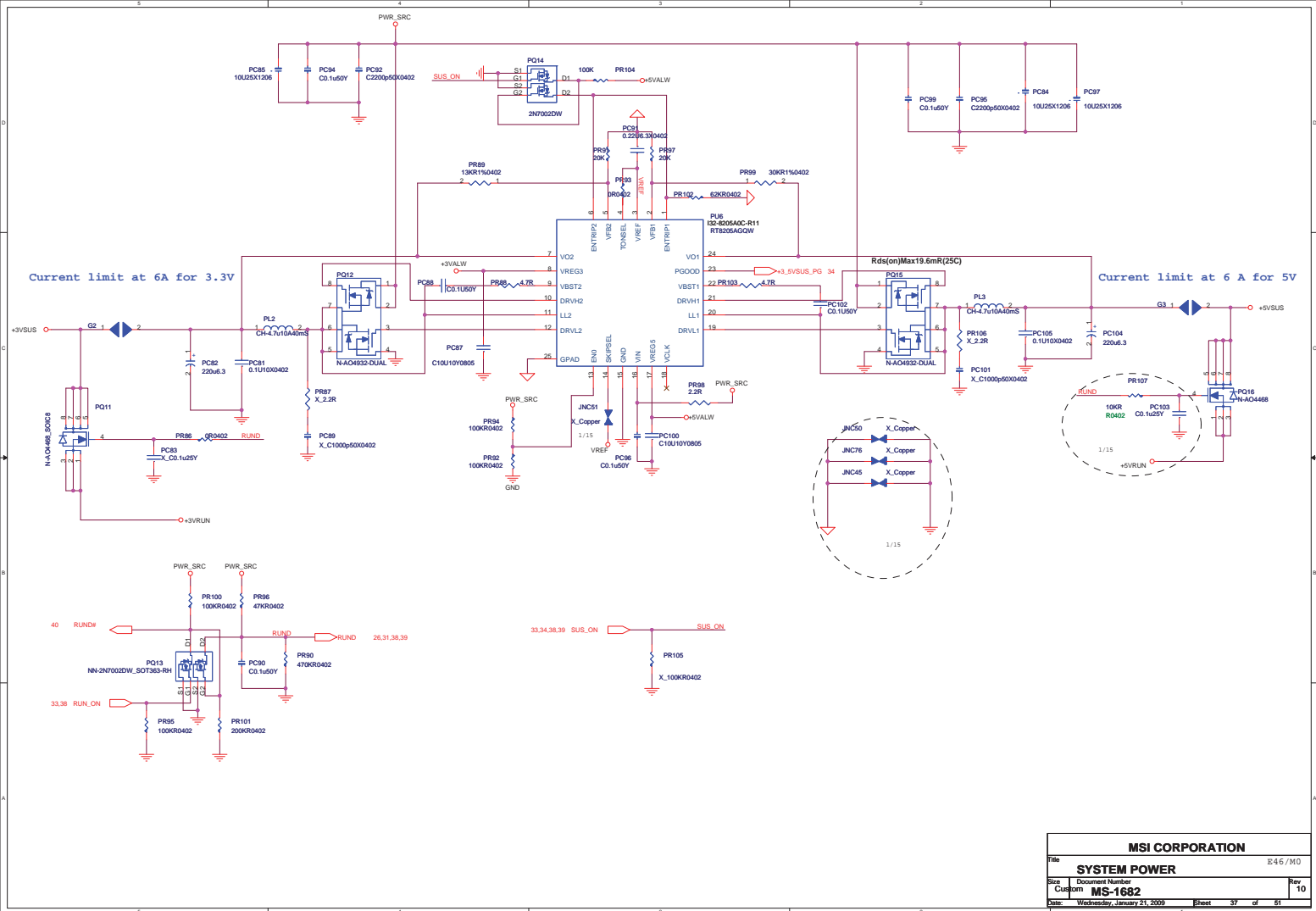
Adapter= 90 W $2.048/7.15 \times (53.6+7.15)=17.4V$
 Adapter input voltage set 17.4 Voltage

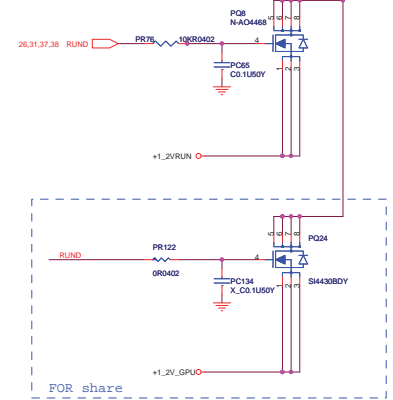
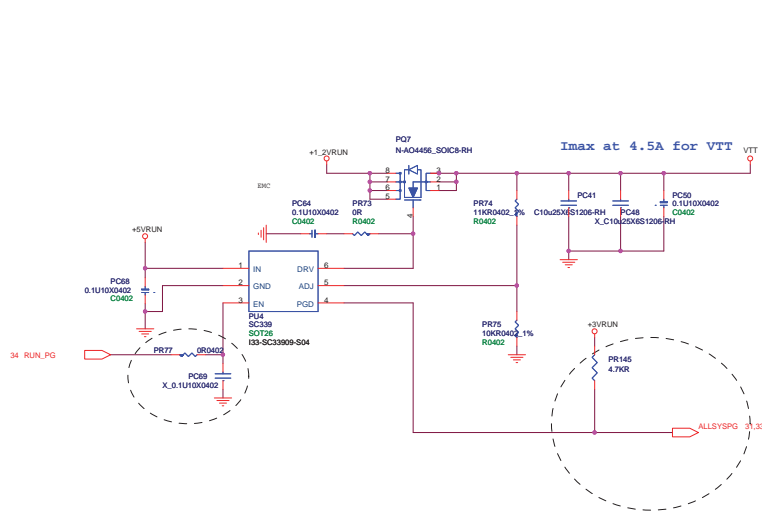
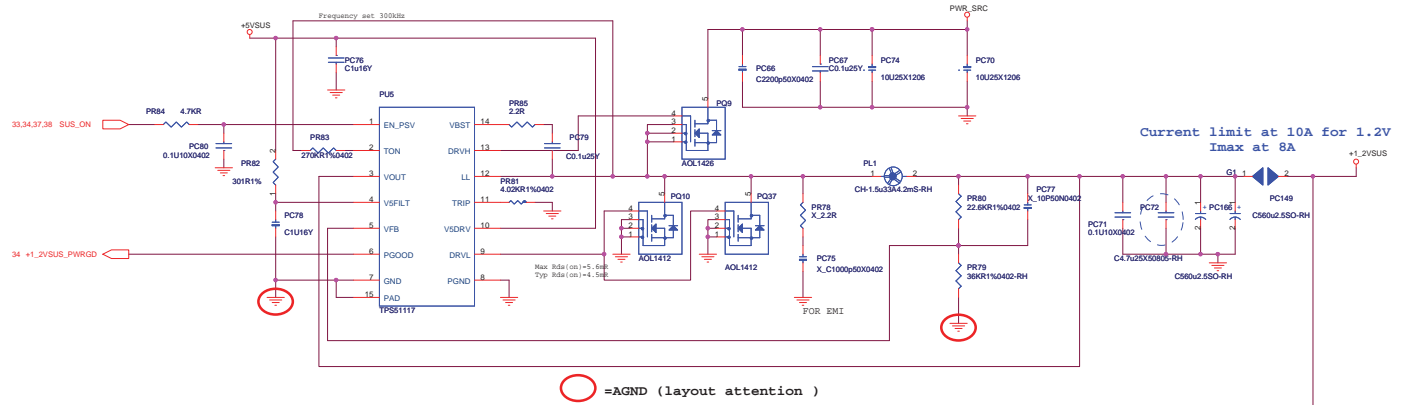


PR85	PR86	
19.1K	28.7K	65W
	24K	75W
	16.9K	90W

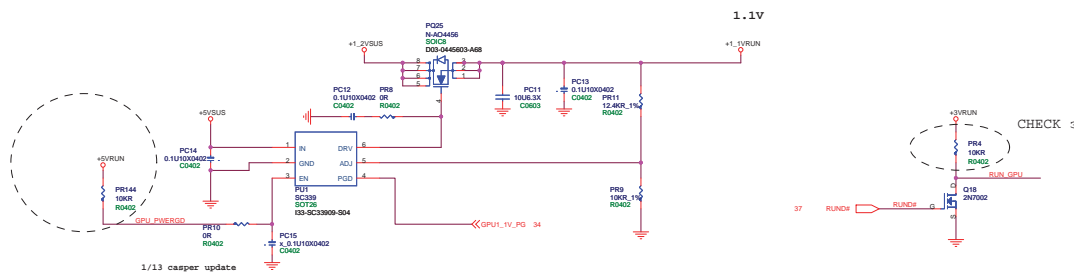
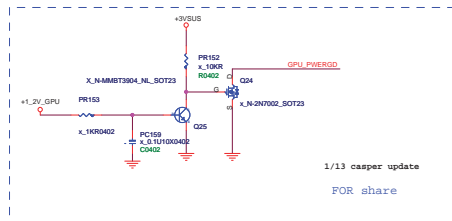
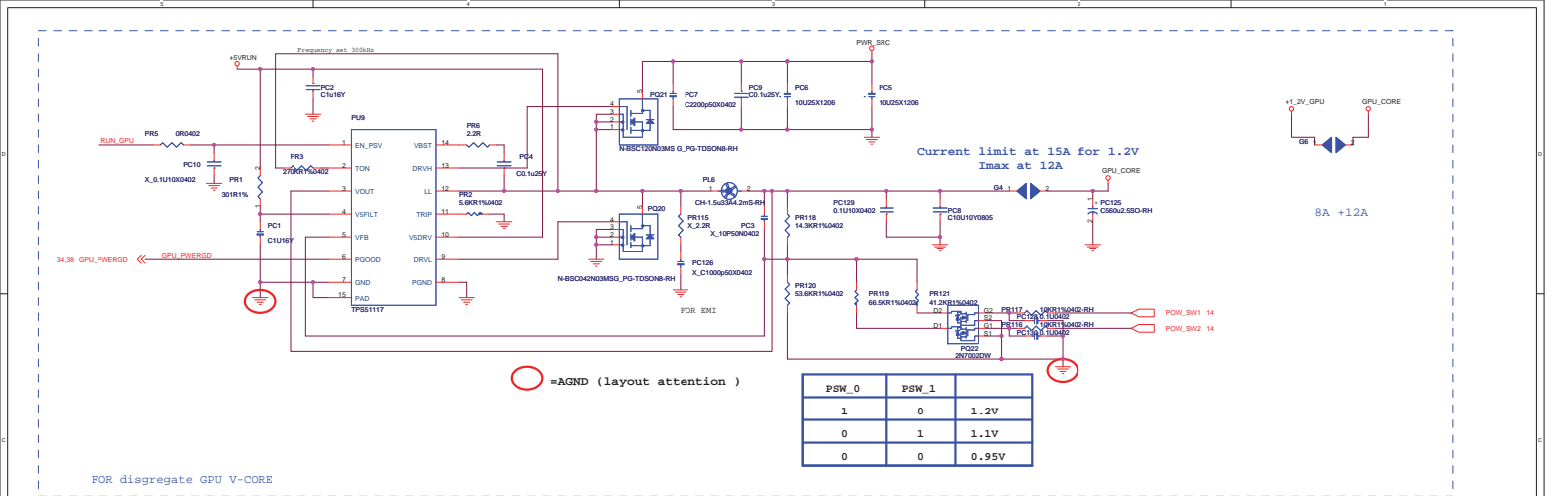
ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

MICRO-STAR INT'L CO.,LTD.			
Battery Charger			
File	Document Number	E51/M0	
Size	Custom	Rev 10	
Date	Wednesday, January 21, 2009 Sheet 35 of 51		



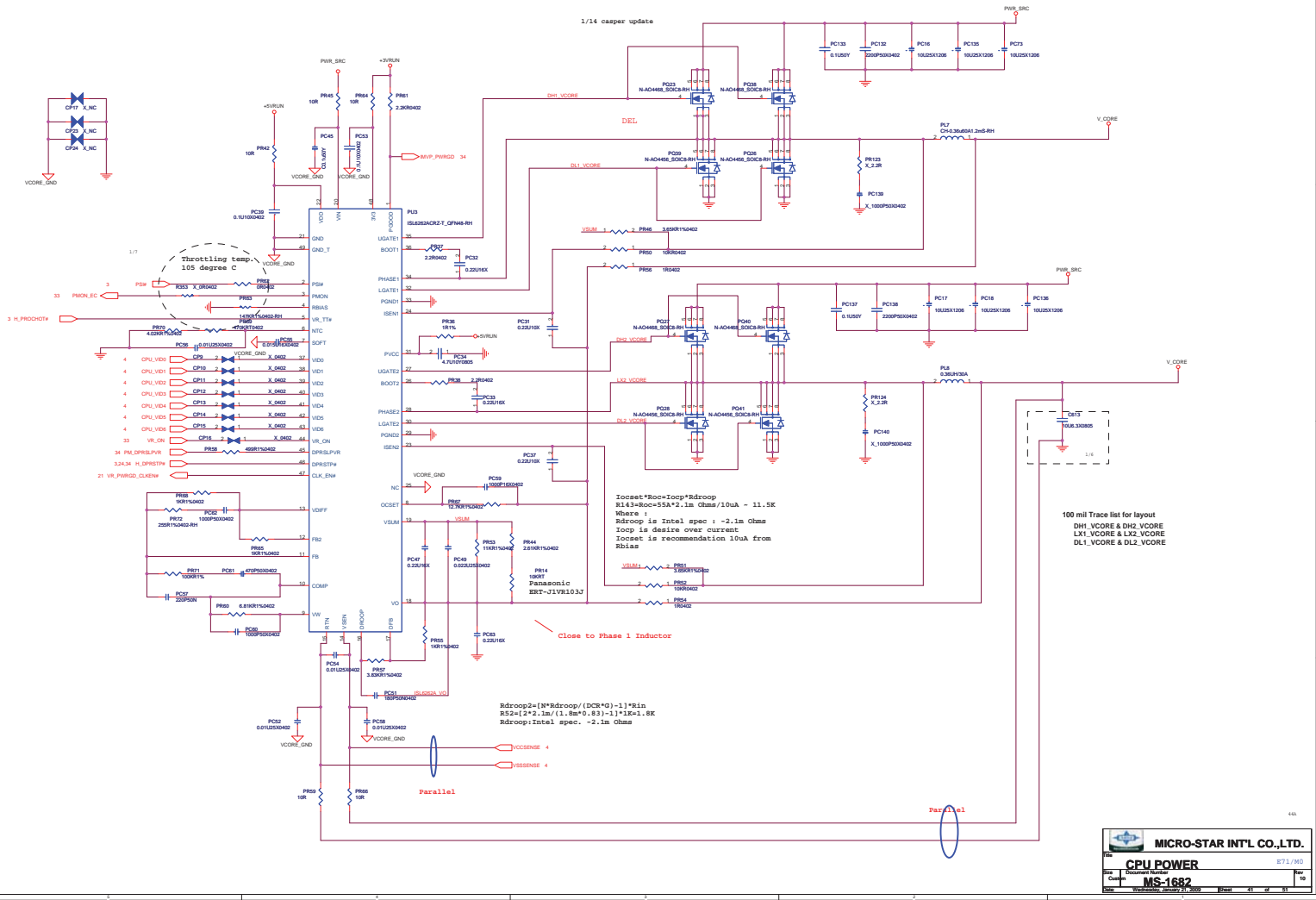


MICRO-STAR INT'L CO.,LTD.			
Title	1.2V & VTT	E3B/M0	
Size	Document Number	MS-1682	
Customer	MS-1682	Rev 10	
Date	Wednesday, January 21, 2009	Sheet	35 of 51

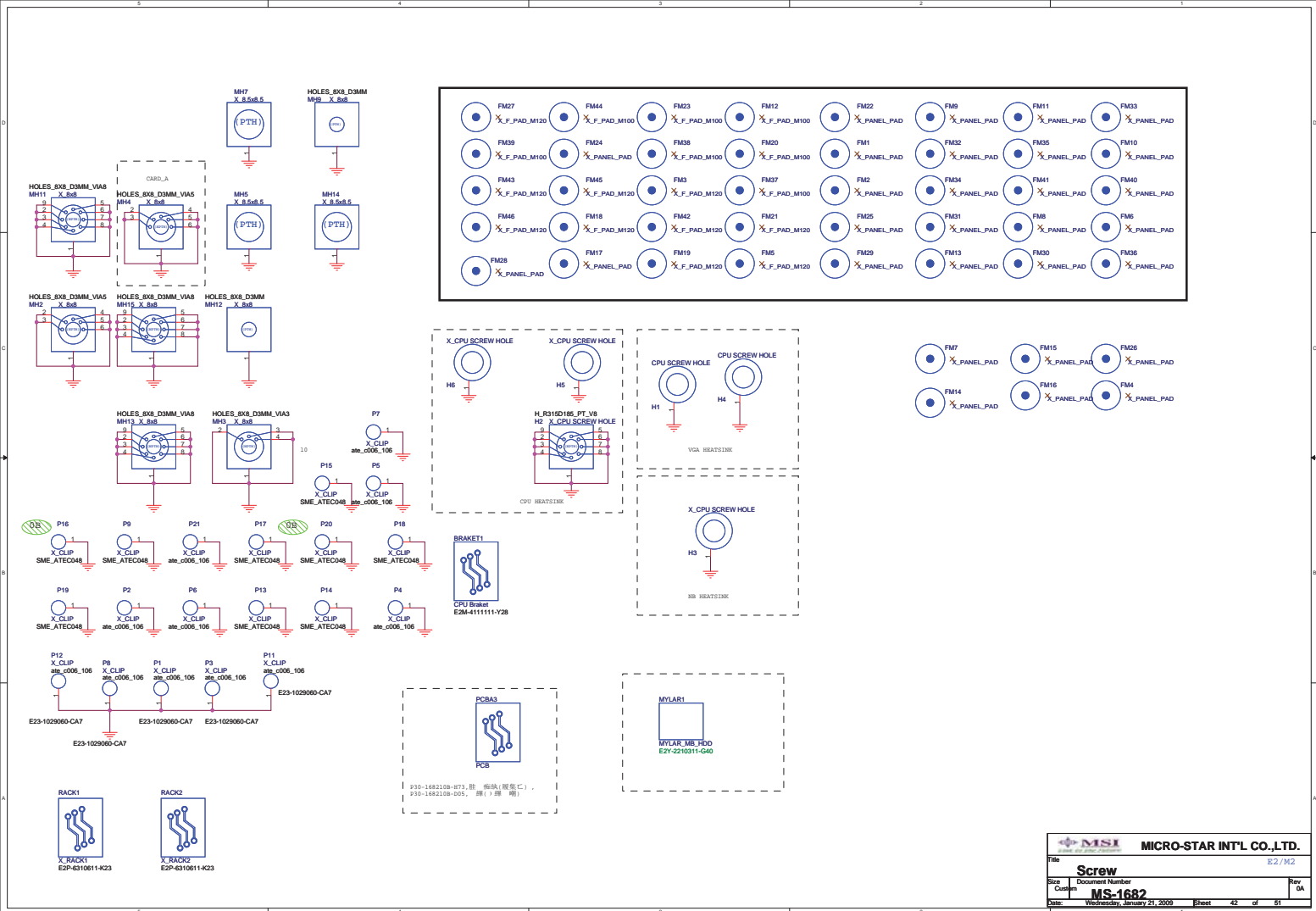


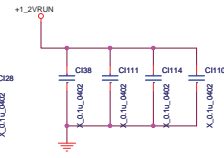
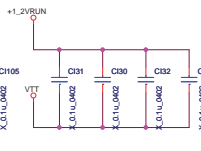
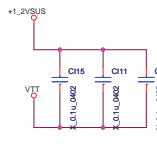
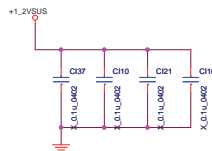
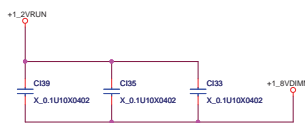
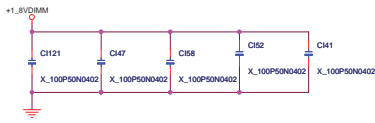
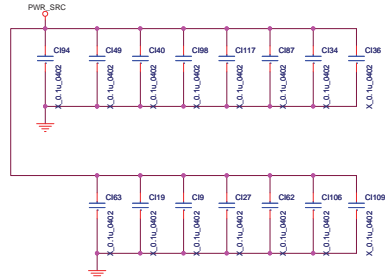
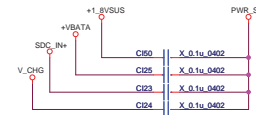
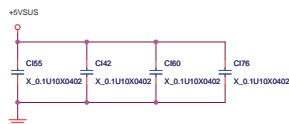
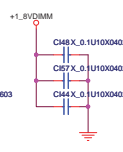
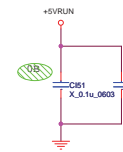
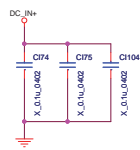
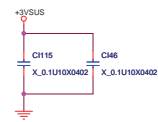
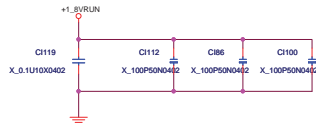
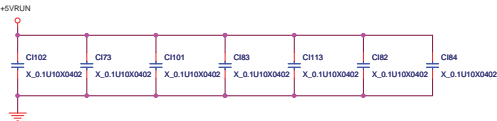
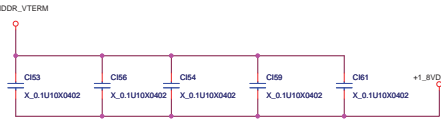
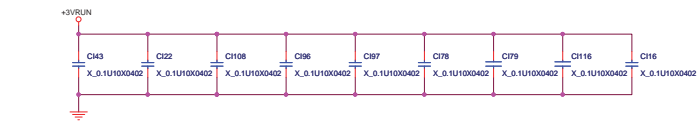
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Size	Document Number	M5-1682
Date	Version	21.000
	Issue	40 of 51


1/14 casper update

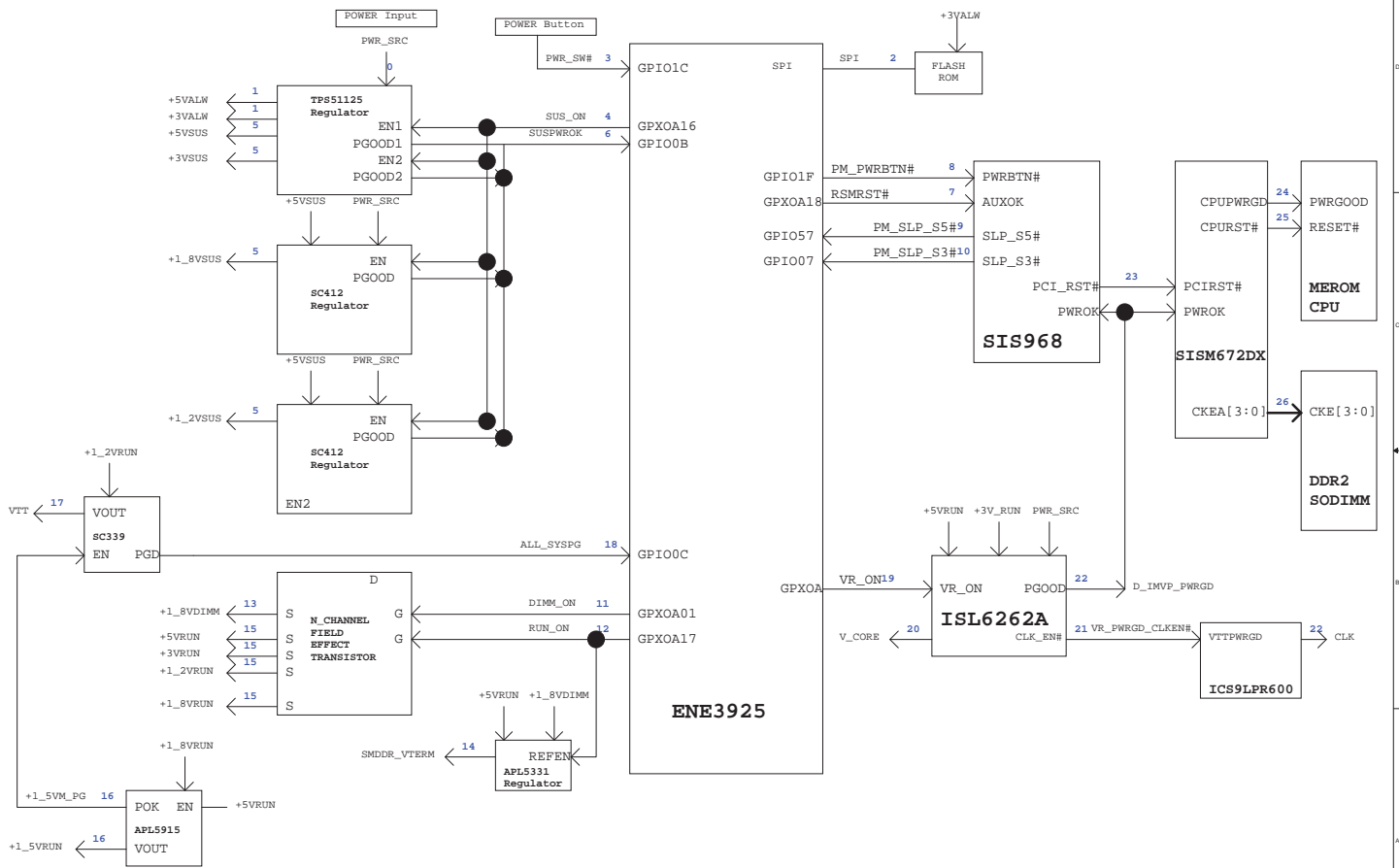


MICRO-STAR INT'L CO., LTD.		ST1/MO
CPU POWER		
Doc No.	MS-1682	Rev 1.0
Date	2014/04/24	Page 41 of 51



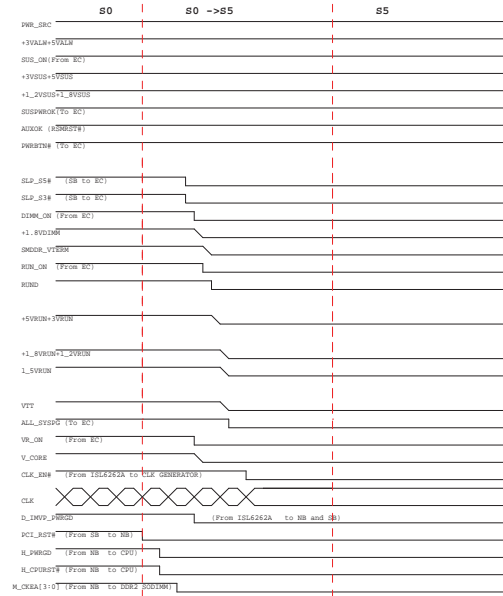


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Custom	MS-1682	0A	
Date	Wednesday, January 21, 2009	Sheet	43 of 51

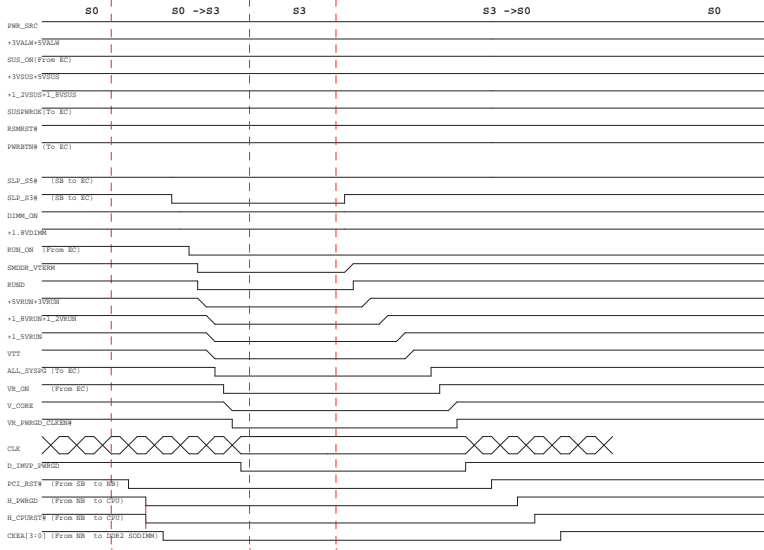


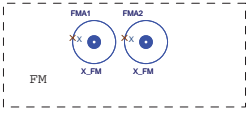
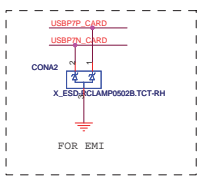
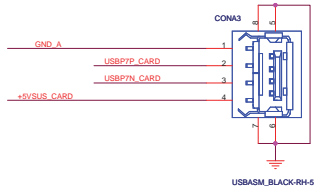
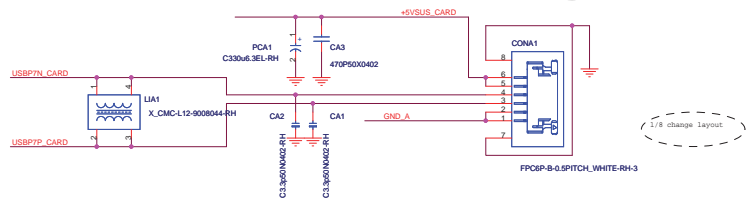
EC programming timing
SiSM672FX + 968 timing SPEC

EC programming timing
SiSM672FX + 968 timing SPEC

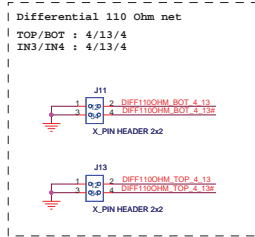
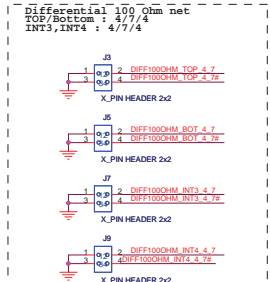
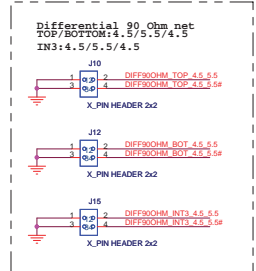
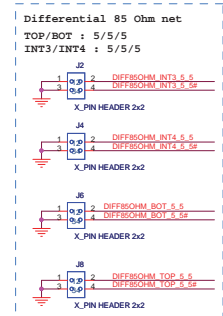
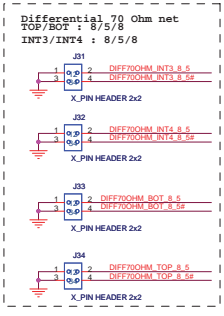
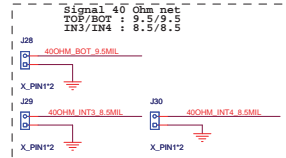
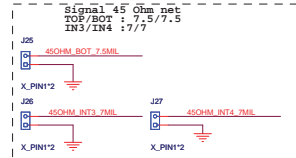
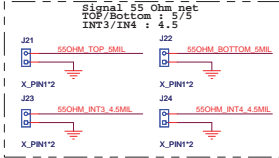
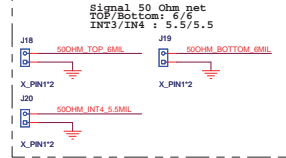
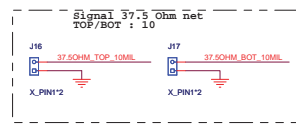


AC S0-S3-S0
EC programming timing
SiSM672FX + 968 timing SPEC





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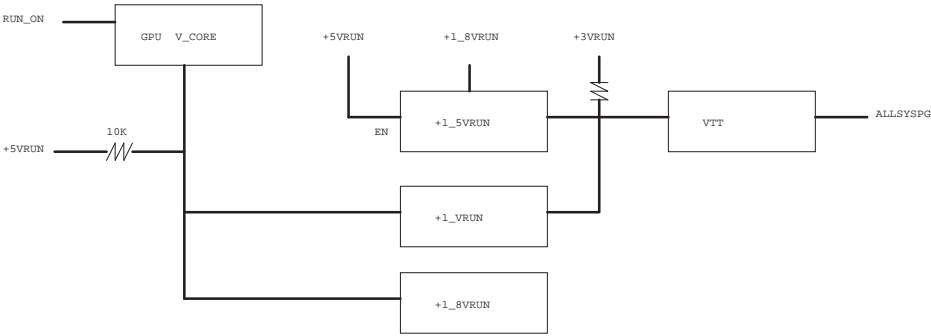
0A -- 0B Note

MS-1682

P03, C579 INSTALL by SA BUG ,R41 CHANGE F/P TO R0603
P04, C639,C623,C612,C640,C624 INSTALL X5R
P06, R322 INSTALL
P07, R177,R171 CHANGE 36R , R170,R176 CHANGE 40.2R ,JNC70,JNC75 CHANGE F/P TO NC_0603
P14, R124,R125,R301 CHANG JNC81,JNC82,JNC83 AND INSTALL , R67,R68 DEL ,ADD PR135,RN28,JNC80,R346 ,R346 CHANGE F/P TO R0603, U5 PIN 8 ,7 CHANGE NET NAME ,JNC29 &R85 CHANGE
P15, C50 INSTALL
P16, R52,R246 INSTALL ,R51,R242 DON'T INSTALL
P18, R225,R227,R13,R14 CHANGE 499R
P19, R223,R224,R12,R11 CHANGE 499R
P20, CHANGE U15 FOOTPRINT TO " SOT23_5_NPC30X " , VGA_DATA AND VGA_CLK AND *J38 : PIN 30 "CHANGE TO +3.3V_DELAY , R232,R233 ,C486,C487,C488 INSTALL
P21, RN14 PIN 2,4 SWAP PIN 6,8
P22, DEL SPI_SKET1,JNC66,JNC67,JNC71,JNC72,CON4 , R318 INSTALL, R317 DON'T INSTALL ,JNC34 ,JNC33 CHANGE F/P TO NC_0603
P23, JNC65,JNC64,JNC59,JNC56,JNC55 INSTALL by SA BUG ,R41 CHANGE F/P TO R0603
P26, CN5 CHANGE CAD, CN6 CHANGE LAYOUT AND PIN 6 TO GND
P27, DEL D1,D2, R212 CHANGE TO +5VSUS
P28, R189 CHANGE 0 Ohm AND INSTALL , CHANGE CON5 PIN 29,20,27 NET NAME, DEL R187,R186 , U12 CHANGE 5159 "B07-0515904-R09 "
P29, Y1 CHANGE F/P, U23 NET CHANGE
P30, JGFS1 DON'T INSTALL, USIM_PWR > 25 mils, DEL SW1,SW2,SW3,SW4,JNC1,2,3,4
P31, R112,D16 TO ALLSYSPG, R115,C212 NOT INSTALL, R108 INSTALL
P32, R290 CHANG TO 33K ,C622 CHANGE TO 4.7U,CON7 SWAP PIN 1 &PIN 2
P33, U20 CHANGE FOOTPRINT SIC8_SST_S2A , CN3 CHANGE NEW PN , DEL R346 TO RUN_PG, U3 PIN 113 CHANGE TO PIN 23 , U3 PIN 98 & PIN 130 SWAP,JNC8 OGANGE R38 , ADD R354 220HM , SW5,SW6 SWAP LAYOUT, YT1 MOVE
P34, JNC19 CHANGE R345 DON'T INSTALL ,J37 CHANGE FOOT PRINT
P36, PR12 360 CHANGE 620 (R11-0621T12-R01) (3pre-charge current), PR16 9.31K CHANGE 28.7K(R11-2872T12-W08) (36-CELL charge current)
P37, PR107 CHANGE 10K ,INSTALL PC103
P38, ADD PQ36 TO DELAY +1.8VRUN, DEL PR135,PC159 , DON'T INSTALL PR114
P39, PU4 PIN4 TO ALLSYSPG ,PR77 CHANGE 0 Ohm, PC69 DON'T INSTALL ,PC72 10uF CHANGE 4.7uF(C11-4753014-W08) (3jitter)
P40, PR4 CHANGE TO 10K Ohm ,PR63 147 CHANGE 147K(R11-1473T12-Y01) ,ADD GPU_PWERGD NET WAY
P41, PR63 CHANGE TO 147K Ohm , ADD R353 DON'T INSTALL ,C613 INSTALL
P42 , H1:P30 , MH1:CHANGE TO 5020
P47 , CONA1 CHANGE LAYOUT

JNC21, JNC80 ㄱ ㄴ
ADD PR144 TO +5VRUN ㄱcheck
ADD PR145 TO +3VRUN ㄱcheck

MSI CORPORATION			
Title Note			
Size	Document Number		Rev
Custom	MS-1682		0A
Date	Wednesday, January 21, 2009		Sheet 60 of 61



MSI CORPORATION			
Title			
Note			
Size	Document Number		Rev
Custom	MS-1682		0A
Date	Wednesday, January 21, 2009		Sheet 01 of 01